SIS3300/SIS3301
65/80/100 MHz
VME FADCs

User Manual

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Version: 3.40 as of 12.08.04

Revision Table:

Revision	Date	Modification
0.01	27.09.00	Generation
1.00	15.01.01	First official release
1.01	17.01.01	Trigger functionality added
1.02	21.01.01	MBLT64 readout
1.03	01.06.01	Bug fix in acquisition register
1.10	01.08.01	**Documentation**: J190 description **Design Version 2 : (added Multiplexer Mode)** - Firmware Revision Register : 0x33000102 - new bit in Acquisition control register (bit 15; MULTIPLEXER Mode) - new Clock Predivider registers - new No_of_Sample registers - new Output 1 function in MULTIPLEXER Mode
2.00	29.10.01	V2 hardware revision, extended functionality
2.10	05.11.01	extended trigger functionality description
2.11	15.11.01	Bug fixes, ADC chip frequency range
3.0x	24.05.02	Prerelease for major functionality/firmware upgrade V3 - implementation of gate chaining mode - introduction of averaging - 2e VME readout implementation - change in trigger bit behaviour Combination of SIS3300 and SIS3301 manual to one document
3.00	27.05.02	Official release
3.01	19.06.02	Removal of side cover for better conduction cooling
3.02	04.07.02	Explanation for single shot/wrap mode
3.10	08.09.02	Further extension of wrap mode description SIS3300/SIS3301 differential input schematic/configuration
3.20	28.10.02	SIS3301 80 MHz
3.30	12.12.02	SIS3301 100 MHz
3.40	12.08.04	Bug fix in clock speed table for SIS3301-80 03 06 firmware for SIS3301 (external clock with delay locked loop)

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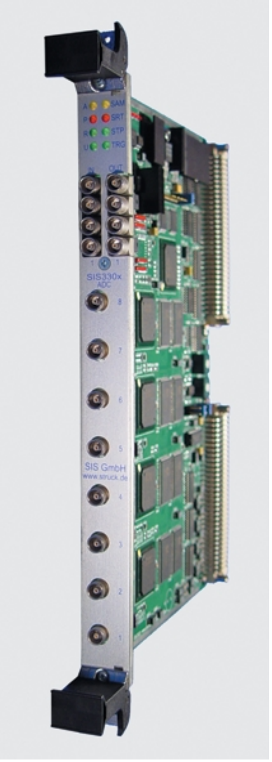
1 Introduction

The SIS3300/3301 are eight channel ADC/digitizer boards with a sampling rate of up to 105 MHz (for the individual channel) and a resolution of 12/14-bit. The boards are single width 6U VME card, which has no special (i.e. non standard VME) voltage requirements.
Dual memory bank functionality in conjunction with multi event memory structure and a range of trigger options give the unit the flexibility to cover a variety of applications.

Applications comprise but are not limited to:

- digitization of “slow” detectors like calorimeters
- spectroscopy with Ge-detecors
- beam profile monitor readout
- serialized readout of µ-Strip detector data



As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm.

1.1 Related documents

A list of available firmware designs can be retrieved from
http://www.struck.de/sis3300firm.htm
The JTAG firmware installation procedure is described in
http://www.struck.de/sis3300_jtagprog.pdf

2 Technical Properties/Features

2.1 Key functionality

Find below a list of key features of the SIS3300 and SIS3301 digitizers.

	SIS3300	SIS3301-65	SIS3301-80	SIS3301-105
Sampling rate per channel	105 MHz	65 MHz	80 MHz	105 MHz
Minimum symmetric clock	1 MHz	15 MHz	15 MHz	15 MHz
Resolution	12-bit	14-bit	14-bit	14-bit
Analog bandwidth	> 80 MHz	35 MHz (1)	40 MHz	70 MHz
Typical pedestal variance	0.7 bit	1.1 bit (2)	1.1 bit (2)	1.1 bit (2)
Differential input version	-	X	X	X
2 x 128 KSample default	X	X	X	X
2 x 512 KSample option	-	X	X	X

(1) limited for better resolution
(2) with symmetric input range

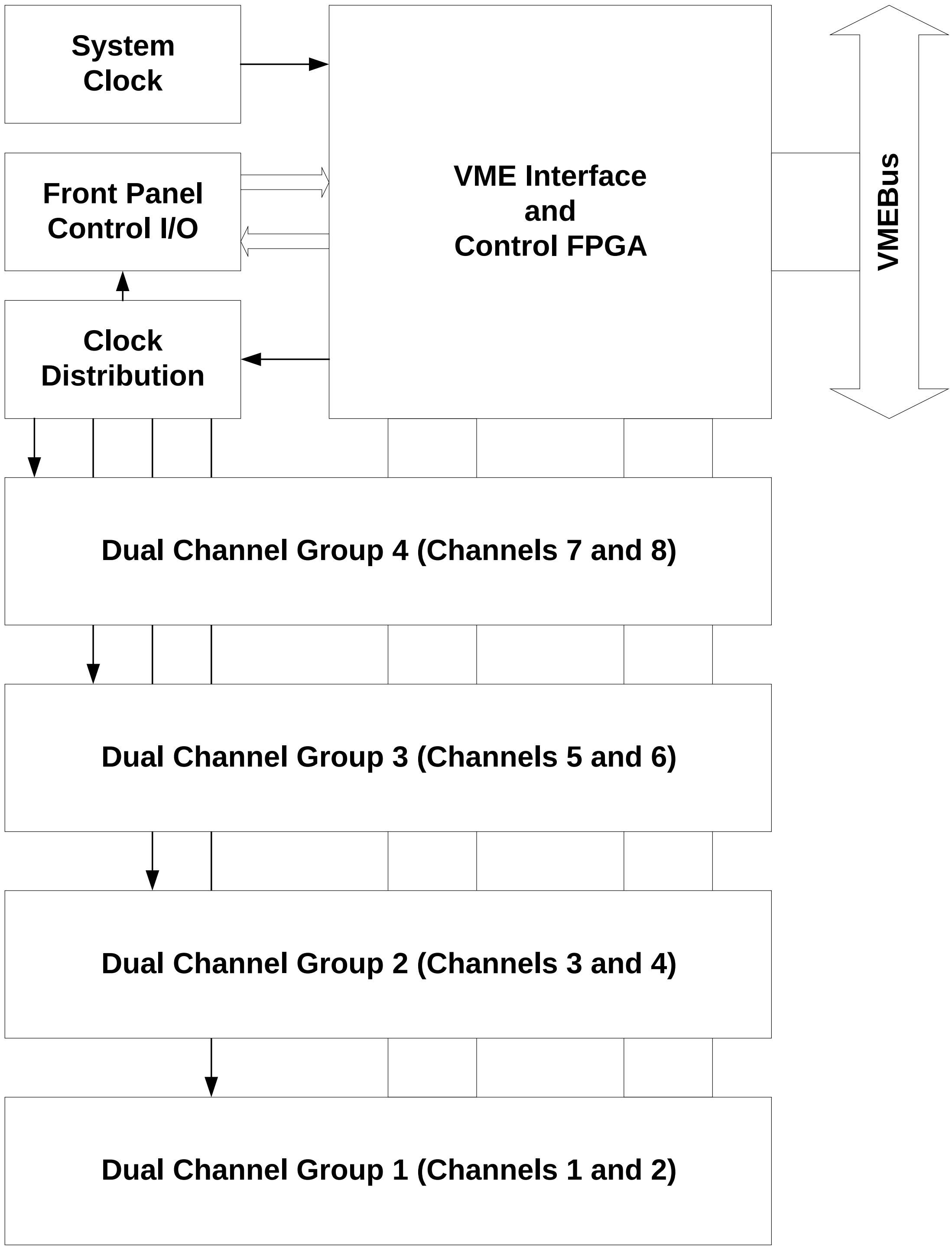
Common properties of all boards are:

- 8 channels
- special clock modes (clock prescaling, external “arbitrary” clock)
- channel to channel crosstalk below noise (i.e. invisible in Fourier spectrum)
- external/internal clock
- multi event mode
- N sample averaging (N= 2,4, 8, ..., 128)
- Read on the fly (actual sample value)
- pre/post trigger option
- Two independent memory banks
- trigger generation
- 4 NIM control inputs/4 NIM control outputs
- A32 D32/BLT32/MBLT64/2eVME
- Geographical addressing mode (in conjunction with VME64x backplane)
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Front panel
- VME64x extractor handles (on request)
- F1002 compatible P2 row A/C assignment
- +5 V, +12V and –12 V VME standard voltages

Note: The SIS3300/1 shall not be operated on P2 row A/C extensions, like VSB e.g. due to the compatibility to the F1001 FADC modules clock and start/stop distribution scheme.

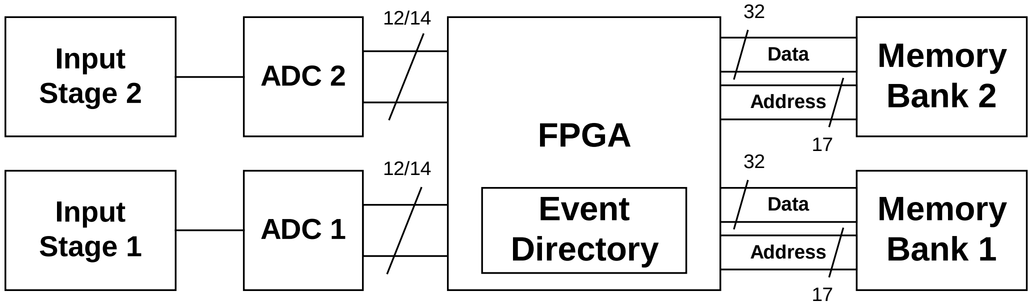
2.2 Module design

The SIS3300 consists of four identical groups of 2 ADC channels and a control section as shown in the simplified block diagram below.



2.2.1 Dual channel group

Two ADC channels form a group, which memory is handled by one Field Programmable Gate Array (FPGA).



2.3 Modes of Operation

The SIS3300 was developed with maximum flexibility in mind. The FPGA based design of the card allows to meet the requirements of many readout applications with dedicated firmware designs in the future. The initial firmware is supposed to furnish you with an easy to use yet powerful high speed high resolution Flash Analog to Digital Converter (FADC) implementation, that covers many everyday analog to digital applications.

2.4 Memory management

The individual memory bank(s) can be used either as one contiguous memory or as a subdivided multi event memory. In addition memory depth can be limited in single event operation to match the requirements of the given application. The memory configuration is defined through the memory configuration register, while bank handling (on dual memory bank modules) is under control of the acquisition control register.

2.4.1 Single Event Mode

The full memory of 128 K Samples of the SIS3300/1 is used as one big circular buffer or as single shot memory in single event mode, unless memory size is limited by the event configuration register.

2.4.2 Multi Event Mode

The memory can be divided in up to 1024 pages or events to make the acquisition of shorter signals more efficient. The stop pointers for the individual page can be retrieved from the event directory. In auto start mode the ADC advances to the next page and starts sampling automatically.

2.4.3 Dual Bank Mode

Dual bank mode (Bank Switch mode) is available on cards (except SIS3300 V1 PCBs). The single/multi event selection will influence both memory banks in the same fashion. Data from the inactive bank can be readout, while the other bank is acquiring new data.

2.5 Clock sources

The SIS3300/3301 features 3 basic clock modes

- Internal clock
- External symmetric clock
- External random clock

2.5.1 Internal clock

The internal clock is generated from an on board 40 or 50 MHz quartz. It is either doubled by a delay locked loop to 80/100 MHz or divided down to lower clock frequencies. The table below lists the valid clock settings for the different SIS3300/3301 boards.

Clock	SIS3300	SIS3301-65	SIS3301-80	SIS3301-105
100 MHz	X	-	-	X
80 MHz	-	-	X	-
50 MHz	X	X	-	X
40 MHz	-	-	X	-
25 MHz	X	X	-	X
20 MHz	-	-	X	-
12.5 MHz	X	-	-	-
6.25 MHz	X	-	-	-
3.125 MHz	X	-	-	-

2.5.2 External clock

A symmetric external clock (NIM level, ratio between 45:55 and 55:45) can be fed to the module through a LEMO00 connector. An ECL clock over rows A/C of the J2 VME backplane can be used as an alternative. For optimum performance the clock frequency should be within the specified range for the given ADC chip.

Module	Min. sym. clock	Max sym. clock
SIS3300	1 MHz	105 MHz
SIS3301-65	15 MHz	65 MHz
SIS3301-80	15 MHz	80 MHz
SIS3301-105	15 MHz	105 MHz

2.5.3 Random External Clock

Random external clock mode allows to operate the SIS3300/1 with basically arbitrary external clock pulse trains or slow external clocks. The module is clocked with the internal clock (typically at 100 MHz) and a data word will be stored to memory upon the next leading edge of the internal clock after a leading edge on the external clock input is detected. Internal pipelining has to be taken into account, the datum will precede the clock by 10 clock ticks (i.e. about 100 ns on a SIS3300 clocking at 100 MHz).

2.6 Averaging

Averaging over N (N=2, 4, 8, ..., 128) consecutive samples can be used to cover the domain of lower speed digitizers with the SIS3300/1 cards without compromising on the resolution/signal to noise ratio side.

2.7 Trigger control (pre/post, start/stop and gate mode)

The SIS3300/1 features pre/post trigger capability as well as start/stop mode acquisition and a gate mode (in which start and stop are derived from the leading and trailing edge of a single control input signal).
The trigger behaviour is defined by the acquisition control register.

2.8 Internal Trigger generation

The trigger output of the SIS3300/1 can be either used to interact with external trigger logic or to base start/stop on a threshold (i.e. one individual threshold per ADC channel) of the digitized data. Trigger generation can be activated with two conditions:

- module armed (i.e. sample clock active, trigger can be used to start acquisition)
- module armed and started (trigger can be used to stop acquisition)

The user can select between triggering on the conditions above and below threshold

2.9 Time Stamp Memory

A 1024 x 24 bit Time Stamp Memory is implemented for each memory bank.
An internal counter starts with the first Stop trigger condition in multievent mode and it will be incremented with the sample clock or with the predivided sample clock (factor 1 to 256).
Each stop trigger condition (end of event) writes the counter value into Time Stamp Memory.

2.10 VME Interrupts

Two registers, the Interrupt configuration and the Interrupt control register, are implemented for interrupt setup and control.
Four Interrupt sources are implemented:

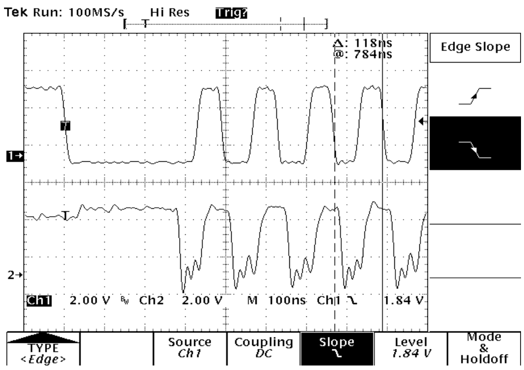
- External User Input (LEMO input 1)
- End of event
- End of last event in multievent mode
- Memory bank full in bank switch mode (Dual bank)

2.11 VME Readout Speed

The VME interface is optimized for readout speed. An internal FIFO/pipeline structure allows for high speed readout in block transfer mode (BLT32, MBLT64, 2eVME).
The timings below were measured with the SIS3100 (VME master) and the SIS3300/SIS3301 (VME Slave). The upper scope trace shows the VME signal DS1* (data strobe, low active). The VME Master asserts the DS1* to request (read) data.
The lower signal shows the VME signal DTACK* (Data Acknowledge, low active). The VME Slave asserts the DTACK* to acknowledge. that the data is valid on VME.

SIS330x DS* to DTACK* : 30-40ns

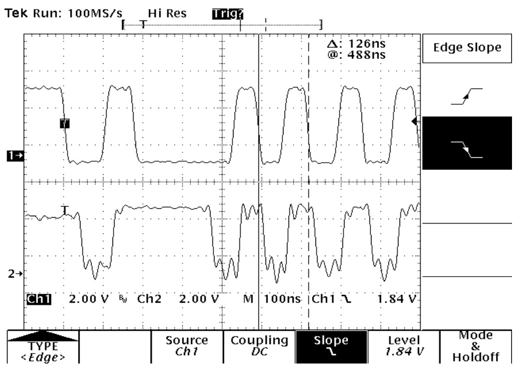
32bit every 120ns -- > ~ **33 MByte/sec**



BLT32

SIS330x DS* to DTACK* : 30-40ns

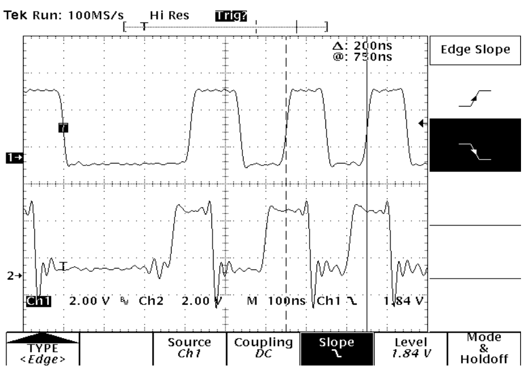
64bit every 125ns -- > ~ **64 MByte/sec**



MBLT64

SIS330x DS* to DTACK* : 50-60ns

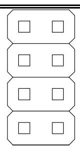
128bit every 200ns --> ~ **80 MByte/sec**



2eVME

3 VME Addressing

As the SIS3300 VME FADC features memory options with up to 2 banks of 4 times 128 K samples each, A32 addressing was implemented as the only option. Hence the module occupies an address space of 0xFFFFFF Bytes (i.e. 16 MBytes) are used by the module.
The SIS3300/1 firmware addressing concept is a pragmatic approach to combine standard rotary switch style settings with the use of VME64x backplane geographical addressing functionality.
The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW1 and SW2 (in non geographical mode).

	Function
J1 	EN_A32
	EN_GEO
	EN_VIPA
	reserved

The table below summarises the possible base address settings.

J1 Setting			Bits							
A32	GEO	VIPA	31	30	29	28	27	26	25	24
x			SW1				SW2			
x	x		0	0	0	GA4	GA3	GA2	GA1	GA0
		x	Not implemented in this design							

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective
GA0-GA4	Geographical address bit as defined by the VME64x(P) backplane

Notes:

- This concept allows the use of the SIS3300/1 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.
- The factory default setting is EN_A32 closed, SW1=3, SW2=0 (i.e. the module will react to A32 addressing under address 0x30000000)
- Early SIS3300 boards (PCB SIS3300_V1) have a different base address scheme

3.1 Address Map

The SIS3300 resources and their locations are listed in the table below.
Note: Write access to a key address (KA)with arbitrary data invokes the respective action

Offset	Size in Bytes	BLT	Access	Function
0x00000000	4	-	W/R	Control/Status Register (J-K register)
0x00000004	4	-	R	Module Id. and Firmware Revision register
0x00000008	4	-	R/W	Interrupt configuration register
0x0000000C	4	-	R/W	Interrupt control register
0x00000010	4	-	R/W	Acquisition control/status register (J-K register)
0x00000014	4	-	R/W	Extern Start Delay register
0x00000018	4	-	R/W	Extern Stop Delay register
0x0000001C	4	-	R/W	Time stamp predivider register
0x00000020	4	-	KA W	General Reset
0x00000030	4	-	KA W	VME Start sampling
0x00000034	4	-	KA W	VME Stop sampling
0x00000040	4	-	KA W	Start auto bank switch
0x00000044	4	-	KA W	Stop auto bank switch
0x00000048	4	-	KA W	Clear bank 1 memory full
0x0000004C	4	-	KA W	Clear bank 2 memory full
0x00000060	4	-	R/W	One wire Id. Register (SIS3301 V3.05 only)
0x00001000	0x1000	BLT32	R	Event Time Stamp directory bank 1
0x00002000	0x1000	BLT32	R	Event Time Stamp directory bank 2
Event information all ADC groups				
0x00100000	4	-	W only	Event configuration register (all ADCs)
0x00100004	4		W only	Trigger Threshold register (all ADCs)
0x0010001C	4	-	W only	Trigger Flag Clear Counter register (all ADCs)
0x00100020	4	-	W only	Clock Predivider register (all ADCs)
0x00100024	4		W only	No_Of_Sample register (all ADCs)
0x00100028	4		W only	Trigger setup register (all ADCs)
0x0010002C	4		W only	Max. No of Events register (all ADCs)
0x00101000	0x1000	BLT32	R	Event directory bank 1 (all ADCs)
0x00102000	0x1000	BLT32	R	Eevent directory bank 2 (all ADCs)
Event information ADC group 1				
0x00200000	4	-	R/W	Event configuration register (ADC1, ADC2)
0x00200004	4		R/W	Trigger Threshold register (ADC1, ADC2)
0x00200008	4	-	R	Bank1 address counter (ADC1, ADC2)
0x0020000C	4	-	R	Bank2 address counter (ADC1, ADC2)
0x00200010	4	-	R	Bank1 Event counter (ADC1, ADC2)
0x00200014	4	-	R	Bank2 Event counter (ADC1, ADC2)
0x00200018	4	-	R	Actual Sample Value (ADC1, ADC2)
0x0020001C	4	-	R/W	Trigger Flag Clear Counter register (ADC1, ADC2)
0x00200020	4	-	R/W	Clock Predivider register (ADC1, ADC2)
0x00200024	4	-	R/W	No_Of_Sample register (ADC1, ADC2)
0x00200028	4		R/W	Trigger setup register (ADC1, ADC2)
0x0020002C	4		R/W	Max. No of Events register (ADC1, ADC2)
0x00201000	0x1000	BLT32	R	Event directory bank 1 (ADC1, ADC2)
0x00202000	0x1000	BLT32	R	Event directory bank 2 (ADC1, ADC2)
Event information ADC group 2				

0x00280000	4	-	R/W	Event configuration register (ADC3, ADC4)
0x00280004	4		R/W	Trigger Threshold register (ADC3, ADC4)
0x00280008	4	-	R	Bank1 address counter (ADC3, ADC4)
0x0028000C	4	-	R	Bank2 address counter (ADC3, ADC4)
0x00280010	4	-	R	Bank1 Event counter (ADC3, ADC4)
0x00280014	4	-	R	Bank2 Event counter (ADC3, ADC4)
0x00280018	4	-	R	Actual Sample Value (ADC1, ADC2)
0x0028001C	4	-	R/W	Trigger Flag Clear Counter register (ADC1, ADC2)
0x00280020	4	-	R/W	Clock Predivider register (ADC3, ADC4)
0x00280024	4	-	R/W	No_Of_Sample register (ADC3, ADC4)
0x00280028	4		R/W	Trigger setup register (ADC3, ADC4)
0x0028002C	4		R/W	Max. No of Events register (ADC3, ADC4)
0x00281000	0x1000	BLT32	R	Event directory bank 1 (ADC3, ADC4)
0x00282000	0x1000	BLT32	R	Event directory bank 2 (ADC3, ADC4)
Event information ADC group 3				
0x00300000	4	-	R/W	Event configuration register (ADC5, ADC6)
0x00300004	4		R/W	Trigger Threshold register (ADC5, ADC6)
0x00300008	4	-	R	Bank1 address counter (ADC5, ADC6)
0x0030000C	4	-	R	Bank2 address counter (ADC5, ADC6)
0x00300010	4	-	R	Bank1 Event counter (ADC5, ADC6)
0x00300014	4	-	R	Bank2 Event counter (ADC5, ADC6)
0x00300018	4	-	R	Actual Sample Value (ADC1, ADC2)
0x0030001C	4	-	R/W	Trigger Flag Clear Counter register (ADC1, ADC2)
0x00300020	4	-	R/W	Clock Predivider register (ADC5, ADC6)
0x00300024	4	-	R/W	No_Of_Sample register (ADC5, ADC6)
0x00300028	4		R/W	Trigger setup register (ADC5, ADC6)
0x0030002C	4		R/W	Max. No of Events register (ADC5, ADC6)
0x00301000	0x1000	BLT32	R	Event directory bank 1 (ADC5, ADC6)
0x00302000	0x1000	BLT32	R	Event directory bank 2 (ADC5, ADC6)
Event information ADC group 4				
0x00380000	4	-	R/W	Event configuration Register (ADC7, ADC8)
0x00380004	4		R/W	Trigger Threshold register (ADC7, ADC8)
0x00380008	4	-	R	Bank1 address counter (ADC7, ADC8)
0x0038000C	4	-	R	Bank2 address counter (ADC7, ADC8)
0x00380010	4	-	R	Bank1 Event counter (ADC7, ADC8)
0x00380014	4	-	R	Bank2 Event counter (ADC7, ADC8)
0x00380018	4	-	R	Actual Sample Value (ADC7, ADC8)
0x0038001C	4	-	R/W	Trigger Flag Clear Counter register (ADC1, ADC2)
0x00380020	4	-	R/W	Clock Predivider register (ADC7, ADC8)
0x00380024	4	-	R/W	No_Of_Sample register (ADC7, ADC8)
0x00380028	4		R/W	Trigger setup register (ADC7, ADC8)
0x0038002C	4		R/W	Max. No of Events register (ADC7, ADC8)
0x00381000	0x1000	BLT32	R	Event directory bank 1 (ADC7, ADC8)
0x00382000	0x1000	BLT32	R	Event directory bank 2 (ADC7, ADC8)
Bank 1 memory				
0x00400000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC1, ADC2)
0x00480000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC3, ADC4)
0x00500000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC5, ADC6)
0x00580000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 1 memory (ADC7, ADC8)

Bank 2 memory				
0x00600000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC1, ADC2)
0x00680000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC3, ADC4)
0x00700000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC5, ADC6)
0x00780000	0x80000	BLT32/MBLT64/2eVME	R/W*	Bank 2 memory (ADC7, ADC8)

*W in D32 only (for memory test e.g.)

Note 1: The event information is identical for the four ADC groups (unless the module has a hardware problem), hence it will be sufficient for normal operation to retrieve the needed information from one group only.

Note 2: MBLT64 and 2eVME read access is supported from the memory banks only.

4 Register Description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3300_CONTROL_STATUS      0x0    /* read/write; D32 */
```

refers to the sis3300.h header file.

4.1 Control/Status Register(0x, write/read)

```
#define SIS3300_CONTROL_STATUS      0x0    /* read/write; D32 */
```

The control register is in charge of the control of basic properties of the SIS3300/1 board, like output signal assignment, in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	write Function	read Function
31	Clear reserved 15 (*)	
30	Clear reserved 14 (*)	
29	Clear reserved 13 (*)	
28	Clear reserved 12 (*)	
27	Clear reserved 11 (*)	
26	clear bank full pulse to output 3 (*)	
25	clear bank full pulse to output 2 (*)	
24	clear bank full pulse to output 1 (*)	
23	Clear reserved 7 (*)	
22	Disable internal trigger routing (*)	
21	Activate trigger upon armed (*)	
20	Non inverted trigger output (*)	
19	Disable reserved 3 (*)	Status P2_SAMPLE_IN
18	Enable user output/disable trigger output (*)	Status P2_RESET_IN
17	Clear user output (*)	Status P2_TEST_IN
16	Switch off user LED (*)	Status User Input
15	Set reserved 15	Status Control 15
14	Set reserved 14	Status Control 14
13	Set reserved 13	Status Control 13
12	Set reserved 12	Status Control 12
11	Set reserved 11	Status Control 11
10	set bank full pulse to output 3	Status Bank full pulse on LEMO output 3
9	set bank full pulse to output 2	Status Bank full pulse on LEMO output 2
8	set bank full pulse to output 1	Status Bank full pulse on LEMO output 1 (highest priority)
7	Set reserved 7	Status Control 7
6	Enable internal trigger routing	Status trigger routing (1= to input, 0=don't route)
5	Activate trigger upon armed and started	Status trigger generation (1=armed and started, 0=armed)
4	Invert trigger output	Status trigger output inversion(1=inverted, 0=straight)

3	Enable reserved 3	Status reserved
2	Enable trigger output/disable user output	multiplexer mode = 0: Status of user/trigger output (1=trigger output, 0=user output) multiplexer mode = 1: output set by multiplexer out pulse
1	Set user output (if bit 2 is not set)	Status User Output (1=output on, 0=output off)
0	Switch on user LED	Status User LED (1=LED on, 0=LED off)

(*) denotes power up default setting

4.1.1 Trigger activation

Trigger generation can be activated for two states of the SIS3300/1. By default trigger generation is active as soon as the module is armed (i.e. a sample clock is active). In this mode the trigger can be used to start the digitizer (with stop condition end of event e.g.). Trigger generation upon armed and started (i.e. bit 6 of the control register set), the trigger is used to stop the module (what is a efficient mode of operation in conjunction with autostart e.g.).

4.1.2 Trigger routing

The trigger status is present on LEMO output 1 (with user output and multiplexer mode disabled). It can be used to form a general trigger decision with external trigger electronics, which is fed back to the corresponding input (start/stop) on the digitizer(s). The trigger is routed on board to the stop input with the internal trigger routing bit set.

4.2 Module Id. and Firmware Revision Register (0x4, read)

```
#define SIS3300_MODID            0x4      /* read only; D32 */
```

This register reflects the module identification of the SIS3300/1 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	3
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	0
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	0/1
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

4.2.1 Major revision numbers

Find below a table with major revision numbers used to date

Major revision number	Application/user
0x01 to 0x0F	Generic designs
0x10	Amanda

4.3 Interrupt configuration register (0x8)

```
#define SIS3300_IRQ_CONFIG      0x8      /* read/write; D32 */
```

This read/write register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.
The interrupter type is DO8 .

4.3.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.
In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again. ROAK IRQ mode can be used in conjunction with the University of Bonn LINUX Tundra Universe II driver by Dr. Jürgen Hannappel on Intel based VME SBCs.

Bit	Function	Default
31		0
...		0
16		0
15		0
14		0
13		0
12	RORA/ROAK Mode (0: RORA; 1: ROAK)	0
11	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	0
10	VME IRQ Level Bit 2	0
9	VME IRQ Level Bit 1	0
8	VME IRQ Level Bit 0	0
7	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	0
6	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	0
5	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	0
4	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	0
3	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	0
2	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	0
1	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	0
0	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	0

The power up default value reads 0x 00000000

4.4 Interrupt control register (0xC)

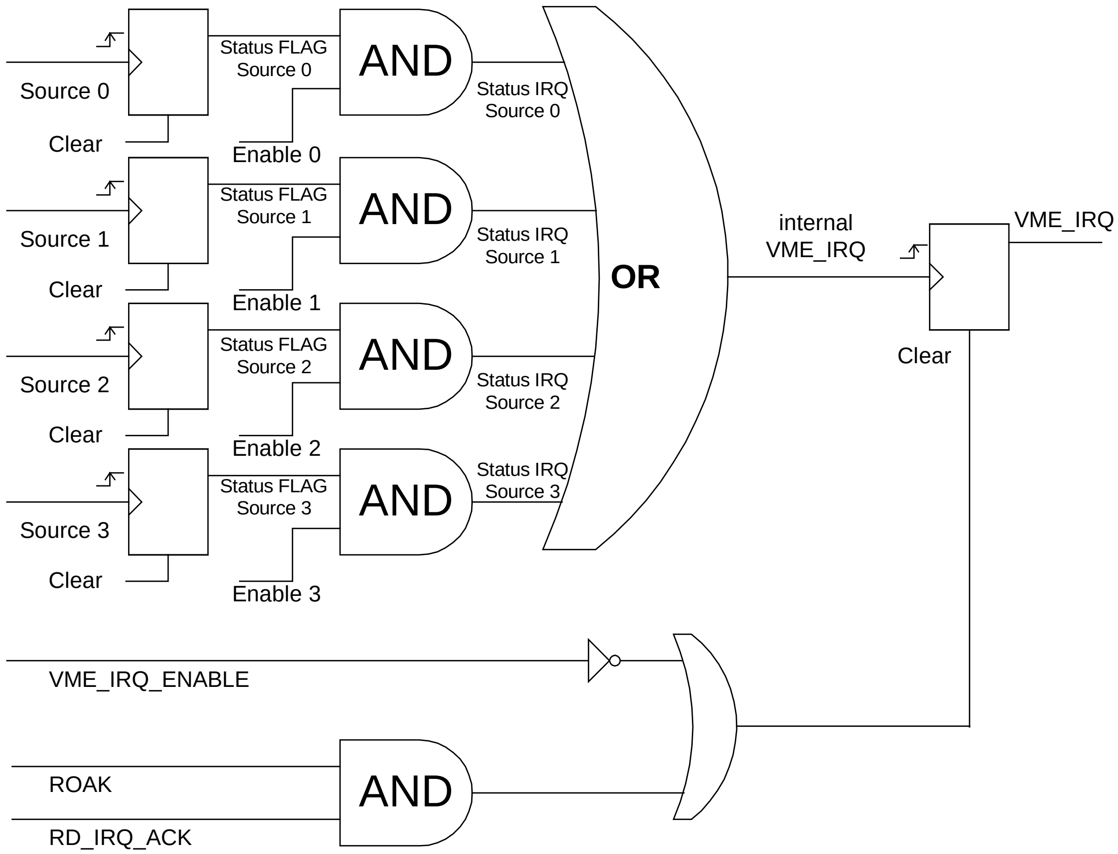
```
#define SIS3300_IRQ_CONTROL          0xC      /* read/write; D32 */
```

This register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.

Bit	Function (w)	(r)	Default
31	unused	Status IRQ source 3 (user input)	0
30	unused	Status IRQ source 2 (reserved)	0
29	unused	Status IRQ source 1 (end of last event, bank full)	0
28	unused	Status IRQ source 0 (end of event)	0
27	unused	Status VME IRQ	0
26	unused	Status internal IRQ	0
25	unused	0	0
24	unused	0	0
23	Clear IRQ source 3	Status flag source 3	0
22	Clear IRQ source 2	Status flag source 2	0
21	Clear IRQ source 1	Status flag source 1	0
20	Clear IRQ source 0	Status flag source 0	0
19	Disable IRQ source 3	0	0
18	Disable IRQ source 2	0	0
17	Disable IRQ source 1	0	0
16	Disable IRQ source 0	0	0
15	unused	0	0
14	unused	0	0
13	unused	0	0
12	unused	0	0
11	unused	0	0
...	...	...	0
4	unused	0	0
3	Enable IRQ source 3	Status enable source 3 (read as 1 if enabled, 0 if disabled)	0
2	Enable IRQ source 2	Status enable source 2 (read as 1 if enabled, 0 if disabled)	0
1	Enable IRQ source 1	Status enable source 1 (read as 1 if enabled, 0 if disabled)	0
0	Enable IRQ source 0	Status enable source 0 (read as 1 if enabled, 0 if disabled)	0

The power up default value reads 0x 00000000

The generation of the status flags, the IRQ flags and the actual IRQ is illustrated with the schematic below:



4.5 *Acquisition control register (0x10, read/write)*

```
#define SIS3300_ACQUISTION_CONTROL    0x10      /* read/write; D32 */
```

The acquisition control register is in charge of most of the settings related to the actual configuration of the digitization process.
Like the control register it is implemented in a J/K fashion.

Bit	Write Function	Read
31	Clear multiplexer mode	0
30	Clear Clock Source Bit2	0
29	Clear Clock Source Bit1	0
28	Clear Clock Source Bit0	0
27	Disable external clock random mode	0
26	Disable front panel gate mode (not start/stop)	0
25	Disable P2 Start/Stop logic	0
24	Disable front panel LEMO start/stop logic	0
23	Disable external stop delay	Bank 2 full
22	Disable external start delay	Bank 2 busy
21	Disable multi event mode 0 : Enable sample clock will be cleared with end of event 1 : Enable sample clock will be cleared at end of bank only (i.e. with last page of memory)	Bank 1 full
20	Disable Autostart (in multi event mode only)	Bank 1 busy
19	Switch off delay locked loop for external clock (SIS3301 03 06 only)	0
18	Disable auto bank switch mode	Bank switch busy
17	Disable sample clock for memory bank 2 (disarm sampling)	0
16	Disable sample clock for memory bank 1 (disarm sampling)	ADC_BUSY
15	Set multiplexer mode	Status multiplexer mode
14	Set clock source Bit 2	Status clock source Bit 2
13	Set clock source Bit 1	Status clock source Bit 1
12	Set clock source Bit 0	Status clock source Bit 0
11	Enable external clock random mode	Status external clock random mode
10	Enable front panel gate mode (not Start/Stop)	Status front panel gate mode
9	Enable P2 Start/Stop logic	Status P2 start/stop logic
8	Enable front panel Lemo Start/Stop logic	Status front panel start/stop logic
7	Enable stop delay (value defined by stop delay register)	Status stop delay
6	Enable start delay (value defined by start delay register)	Status start delay
5	Enable multi event mode 0 : Enable Sample Clock will be cleared with end of event 1 : Enable Sample Clock will be cleared at end of bank only (i.e. with last page of memory)	Status multi event mode
4	Enable Autostart (in multi event mode only)	Status Autostart
3	Use delay locked loop for external clock (SIS3301 03 06 only)	Status delay locked loop for external clock
2	Enable auto bank switch mode	Status auto bank switch mode
1	Enable Sample Clock for Memory Bank 2 (arm for sampling)	Status sample clock bank 2
0	Enable Sample Clock for Memory Bank 1 (arm for sampling)	Status sample clock bank 1

The power up default value reads 0x
Clock source bit setting table:

Clock Source Bit2	Clock Source Bit1	Clock Source Bit0	Clock Source
0	0	0	internal 80/100 MHz

0	0	1	internal 40/50 MHz
0	1	0	internal 20/25 MHz
0	1	1	internal 12.5 MHz
1	0	0	internal 6.25 MHz
1	0	1	internal 3.125 MHz
1	1	0	external clock (front panel)
1	1	1	P2-Clock

Refer to the table in section 2.5.2for allowed clock speeds. Lower sampling rates into memory can be accomplished with a sampling clock within the specified range in combination with the clock predivider register in multiplexer mode or random external clock mode.

4.5.1 Delay locked loop for external clock (SIS3301 03 06)

The external clock signal in the range 60-105 MHz (from a SIS3820 clock distributor e.g.) is used to drive a delay locked loop. The delay locked loop output is used as ADC clock.

4.6 Start Delay register (0x14, read/write)

```
#define SIS3300_START_DELAY     0x14      /* read/write; D32 */
```

Pretrigger operation can be implemented via the start delay register in conjunction with front panel start/stop or gate mode operation. The external and autostart start signal (or leading edge of the gate) will be delayed by the value of the register+2 clocks if the external start delay is enabled in the acquisition control register.

Bit	
32	unused, read as 0
...	
16	unused, read as 0
15	START_DELAY_BIT15
..	
..	
0	START_DELAY_BIT0

The power up default value is 0

4.7 Stop Delay register (0x18, read/write)

```
#define SIS3300_STOP_DELAY      0x18      /* read/write; D32 */
```

Posttrigger operation can be implemented via the stop delay register in conjunction with front panel start/stop or gate mode operation. The external stop signal (or trailing edge of the gate) will be delayed by the value of the register+2 clocks if the stop delay is enabled in the acquisition control register.

Bit	
32	unused, read as 0
...	
16	unused, read as 0
15	STOP_DELAY_BIT15
..	
..	
0	STOP _DELAY_BIT0

The power up default value is 0

Note: The user can generate a gate of defined length (in clock ticks) by fanning a short pulse to the start and stop input with start/stop mode active, stop delay enabled and the stop delay register programmed to the desired gate width. Pipelining will have to be taken into account, i.e. the digitised signal is about 40 ns (with the module sampling at 100 MHz) ahead of the respective control signal, a fact that can be used in external trigger decisions.
For longer external trigger decisions one can consider to pipeline the ADC data in the FPGA in future firmware revisions before storing them to memory.

4.8 Time stamp predivider register (0x1C)

```
#define SIS3300_TIMESTAMP_PREDIVIDER    0x1C      /* read/write; D32 */
```

The (read/write) time stamp predivider register is used to define a prescale factor for the frequency of the time stamp counter. The time stamp counter counts at the clock rate with the time stamp predivider value of 0 and 1, a prescale factor of 2 ... 65535 is selected by writing the corresponding value to the register.

Bit	
31	unused, read as 0
...	
16	unused, read as 0
15	Time stamp predivider BIT15
..	
..	
0	Time stamp predivider BIT0

The power up default value is 0

Note: A predivider value of 0 can not be used with firmware V201

4.9 Key address general reset (0x20, write)

```
#define SIS3300_KEY_RESET                    0x20   /* write only; D32 */
```

A write with arbitrary data to this register (key address) resets the SIS3300 to it's power up state.

4.10 Key address VME start sampling (0x30, write)

```
#define SIS3300_KEY_START                    0x30   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will initiate sampling on the active memory bank if a bank is armed for sampling.

4.11 Key address VME stop sampling (0x34, write)

```
#define SIS3300_KEY_STOP                     0x34   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will halt sampling on the active page. In Single Event Mode or during the last page the sampling this command will halt the the sampling.

To Abort a sampling in Multi Event / Multibank mode the following cycles have to be executed:

- issue "disable autostart" / issue `KEY_STOP_AUTO_BANK_SWITCH`
- issue `SIS3300_KEY_STOP`
- issue clear BX_ENABLE

4.12 Key address start Auto Bank Switch mode (0x40, write)

```
#define SIS3300_KEY_START_AUTO_BANK_SWITCH 0x40  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will start the auto bank switch mode.

4.13 Key address stop Auto Bank Switch mode (0x44, write)

```
#define SIS3300_KEY_STOP_AUTO_BANK_SWITCH  0x44  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will stop the auto bank switch mode.

4.14 Key address clear BANK1 FULL Flag (0x48, write)

```
#define SIS3300_KEY_BANK1_FULL_FLAG        0x48  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the BANK1 FULL Flag.

4.15 Key address clear BANK2 FULL Flag (0x4C, write)

```
#define SIS3300_KEY_BANK2_FULL_FLAG        0x4C  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the BANK2 FULL Flag.

4.16 One wire Id. register 1 (0x60, read/write, SIS3301 V3.05 only)

```
#define SIS3300_ONE_WIRE    0x60        /* read/write; D32;  */
```

A DS2430 256-Bit 1-wire EEPROM can be installed on the SIS3301 to store the serial number of the module. This information is stored in the 64-bit application register of the DS2430 in the factory.

Offset	Contents	Example SIS3301-80 SN 10
0	Module Id.	0x33
1		0x01
2	Clock Speed	0x00
3		0x80
4	Serial Number	0x00
5		0x00
6		0x00
7		0x0A

Note: Module Id. and Clock speed are stored in hexadecimal form for better readability, the serial number is stored as straight 32-bit decimal value.

Refer to the PDF data sheet of the DS2430 and the LINUX example program rom_read.c on the SIS3301 documentation CDROM for details on the operation of the EEPROM.

Bit	Read function	Write function
31	0	not used
...	...	
16	0	not used
15	BUSY	cmd RESET
14	Present	cmd WRITE
13	0	cmd READ
12	0	reserved
11	0	reserved
10	0	reserved
9	reserved	reserved
8	reserved	reserved
7	read datum bit7	write datum bit7
6	read datum bit6	write datum bit6
5	read datum bit5	write datum bit5
4	read datum bit4	write datum bit4
3	read datum bit3	write datum bit3
2	read datum bit2	write datum bit2
1	read datum bit1	write datum bit1
0	read datum bit0	write datum bit0

4.17 Event Time Stamp directory bank 1 (0x1000-0x1ffc, read only)

```
#define SIS3300_EVENT_TIMESTAMP_DIR_BANK1    0x1000
                                        /* read only; D32, BLT32; size: 0x1000 */
```

The event time stamp directory can be used to measure time between triggers (stops) in multi event mode. A scaler counting the ADC clock is enabled with the first stop (hence the time stamp for the first event will read 0 always). The counter value (of the 24-bit wide) scaler is written to the corresponding location for subsequent events.

offset address	Time Stamp (D23:D0)
0x0	Time Stamp 0
..	
0xffc	Time Stamp 1023

4.18 Event Time Stamp directory bank 2 (0x2000-0x2ffc, read only)

```
#define SIS3300_EVENT_TIMESTAMP_DIR_BANK2    0x2000
                                        /* read only; D32, BLT32; size: 0x1000 */
```

As for bank 1.

offset address	Time Stamp (D23:D0)
0x0	Time Stamp 0
..	
0xffc	Time Stamp 1023

4.19 Event configuration registers (0x100000, 0x200000, 0x280000, 0x300000, 0x380000)

```
#define SIS3300_EVENT_CONFIG_ALL_ADC        0x100000   /* write only;D32 */

#define SIS3300_EVENT_CONFIG_ADC12          0x200000   /* read/write;D32 */
#define SIS3300_EVENT_CONFIG_ADC34          0x280000   /* read/write;D32 */
#define SIS3300_EVENT_CONFIG_ADC56          0x300000   /* read/write;D32 */
#define SIS3300_EVENT_CONFIG_ADC78          0x380000   /* read/write;D32 */
```

This register is implemented for each channel group and it has to be written with the same value, the best way is to make use of the address `SIS3300_EVENT_CONFIG_ALL_ADC` to write to the registers of all channel groups simultaneously.

The number of memory divisions (events) is defined by this register in multi event mode. The lowest three bits define the number of memory divisions as listed in the table below. On dual bank units both memory banks will be affected by the configuration of the event configuration register. The maximum number of events is defined by the size of the event directory, which has 1024 entries. The maximum number of events is limited to 65535 in gate chaining mode to allow for shorter gates also.
.

Bit	function
31	unused; read 0
...	...
20	unused; read 0
19	Event_CONF Bit 19 (reserved function)
18	Average Bit 2
17	Average Bit 1
16	Average Bit 0
15	MULTIPLEXER MODE
14	Event_CONF Bit 14 (reserved function)
13	Event_CONF Bit 13 (reserved function)
12	1 (former enable trigger event directory)
11	EXTERNAL CLOCK RANDOM MODE
10	Event_CONF Bit 10 (reserved function)
9	Channel Group ID Bit 1
8	Channel Group ID Bit 0
7	Event_CONF Bit 7 (reserved function)
6	Event_CONF Bit 6 (reserved function)
5	Event_CONF Bit 5 (reserved function)
4	ENABLE_GATE_CHAINING_MODE
3	Enable Wrap around mode (no address auto stop) 0 : Autostop at end of page 1 : Wrap around page until STOP (External or KEY)
2	Page size Bit 2
1	Page size Bit 1
0	Page size Bit 0

The power up default values of the registers are

```
SIS3300_EVENT_CONFIG_ADC12:   0x00001000
SIS3300_EVENT_CONFIG_ADC34:   0x00001100
SIS3300_EVENT_CONFIG_ADC56:   0x00001200
SIS3300_EVENT_CONFIG_ADC78:   0x00001300
```

(i.e. the two channel group ID bits identify the four channel groups)

4.19.1 Gate chaining mode

Gate chaining mode was implemented to allow for effective acquisition of small events of arbitrary length.
Sampling in gate chaining mode will stop when:

- Maximum number of events (see 4.25) is reached
- End of bank is reached, the last event/gate may be incomplete in this case

The first data word of a gate is marked with a 1 in the G(ate) bit in memory (refer to the data format table in section 4.35). For up to 1024 events the information in the event directory is valid also. For gate chaining mode you have to

a.) enable multi event mode
b.) enable gate chaining mode

The deadtime between two gates is 8 clock ticks

Note: the page size (bits 2:0 of the event configuration) are ignored in gate chaining mode as the event size is defined by the gate length of the individual gate pulses (which does not have to be constant).

4.19.2 Averaging mode

Averaging mode is implemented to improve the signal to noise ratio in lower speed digitization applications. N consecutive samples are summed up in the FPGAs of the dual channel groups
Averaging mode is activated by specifying a non zero value for bits 18:16 of the event configuration register(s).

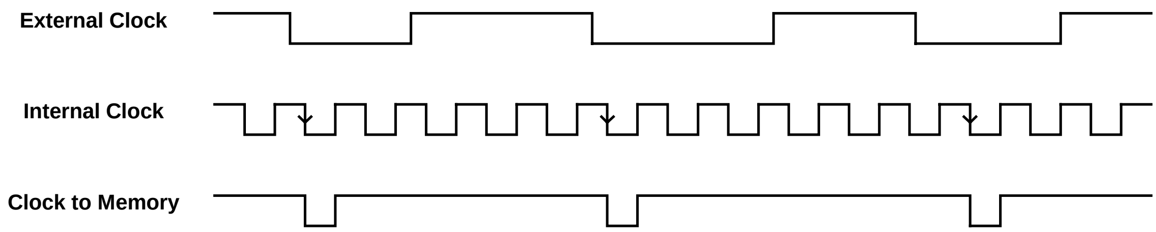
Average Bit 2	Average Bit 1	Average Bit 0	averaged samples
0	0	0	1 (no average)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

4.19.3 MULTIPLEXER MODE

Multiplexer mode was implemented to synchronize data acquisition of the SIS3300/1 with slow external multiplexing hardware. Refer to section 10.1.1 for a description of this acquisition scheme.
Both bit 15 of the acquisition control register and bit 15 of the event configuration register have to be set to acquire data in multiplexer mode.

4.19.4 EXTERNAL RANDOM CLOCK MODE

This mode allows for sampling at arbitrary low and non symmetric external clock. The digitizer is set up for internal clock and will strobe one datum to memory with the leading edge of the internal clock cycle that follows the leading edge of an external clock pulse as illustrated below. Pipelining between the actual analog input signal and the value stored to memory has to be taken into account. Both bit 11 of the acquisition control register and bit 11 of the event configuration register have to be set to acquire data in external random clock mode.



4.19.5 Page size

The page/event size is defined by the 3 page size bits as follows:

Page size Bit 2	Page size Bit 1	Page size Bit 0	Page size	Number of divisions (Events/Bank)
0	0	0	128 K Samples	1
0	0	1	16K Samples	8
0	1	0	4 K Samples	32
0	1	1	2 K Samples	64
1	0	0	1 K Samples	128
1	0	1	512 Samples	256
1	1	0	256 Samples	512
1	1	1	128 Samples	1024

4.20 Threshold registers *(0x100004, 0x200004, 0x280004, 0x300004, 0x380004)*

```
#define SIS3300_TRIGGER_THRESHOLD_ALL_ADC    0x100004  /* write only;D32 */
```

This register is implemented on the base of the individual channel group.
The address `SIS3300_TRIGGER_THRESHOLD_ALL_ADC` can be used to write the same value simultaneously to the registers of all channel groups.

```
#define SIS3300_TRIGGER_THRESHOLD_ADC12      0x200004  /* read/write;D32 */
#define SIS3300_TRIGGER_THRESHOLD_ADC34      0x280004  /* read/write;D32 */
#define SIS3300_TRIGGER_THRESHOLD_ADC56      0x300004  /* read/write;D32 */
#define SIS3300_TRIGGER_THRESHOLD_ADC78      0x380004  /* read/write;D32 */
```

These read/write registers hold the threshold values for the ADC channels 1/3/5/7 and 2/4/6/8.

Via the bits 31 and 15 of the channel group the user can select between greater (GT) or less than/equal as trigger criterion.
GT means: trigger condition is valid if sample data greater then threshold data.

For SIS3300:

Bit	31	30-28	27-16	15	14-12	11-0
Function	0:GT 1:LE	unused	threshold value ADC 1/3/5/7	0:GT 1:LE	unused	threshold value ADC 2/4/6/7

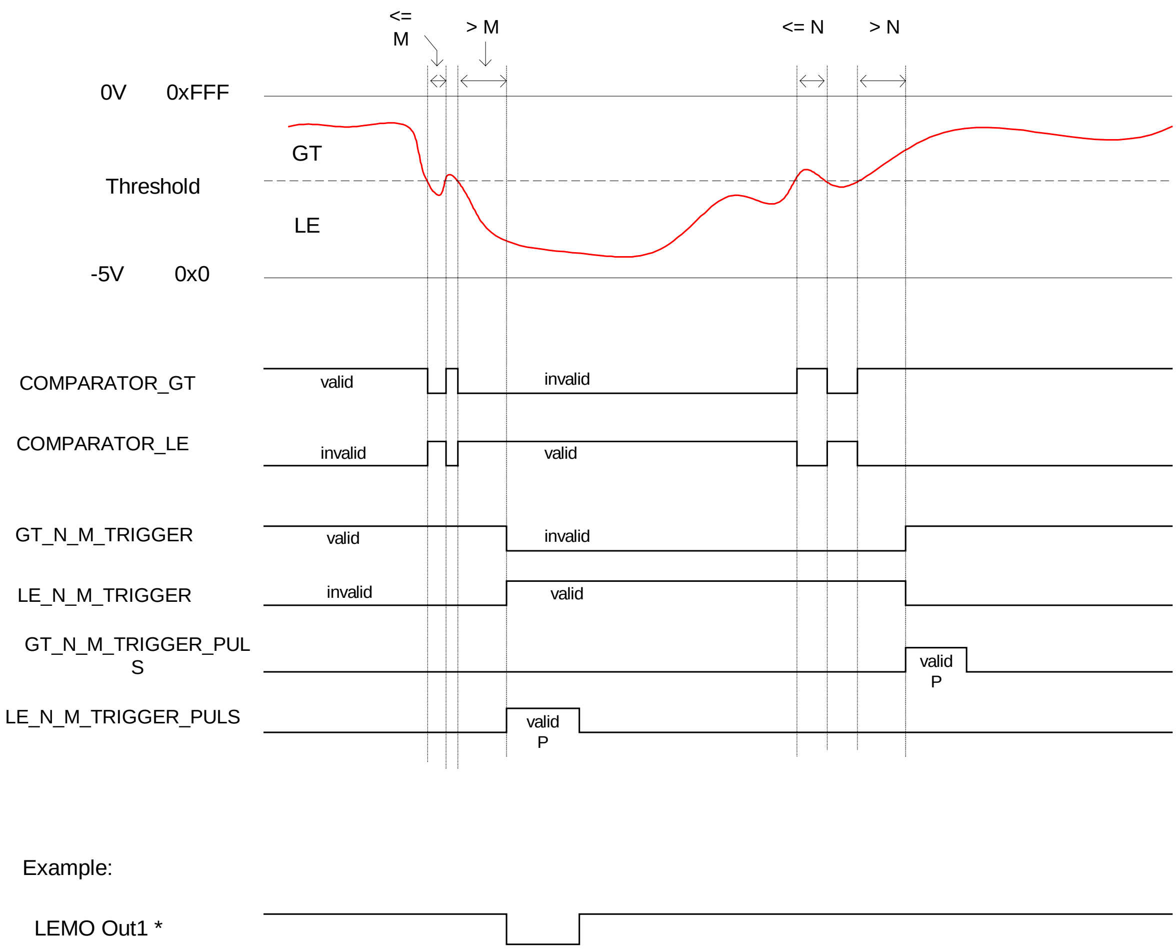
default after Reset: 0x0fff0fff (disable Trigger)

For SIS3301:

Bit	31	30	29-16	15	14	13-0
Function	0:GT 1:LE	unused	threshold value ADC 1/3/5/7	0:GT 1:LE	unused	threshold value ADC 2/4/6/7

default after Reset: 0x3fff3fff

The function of the trigger setup register is illustrated with the drawing below:



4.21 Trigger Flag Clear Counter register (0x10001C, 0x20001C, 0x28001C, 0x3001C, 0x38001C)

```
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ALL_ADC 0x10001C  /* write only;D32 */

#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC12   0x20001C  /* read/write;D32 */
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC34   0x28001C  /* read/write;D32 */
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC56   0x30001C  /* read/write;D32 */
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC78   0x38001C  /* read/write;D32 */
```

This register is implemented on the base of the channel group.
Use the address `SIS3300_TRIGGER_FLAG_CLR_CNT_ALL_ADC` to write to the registers of all channel groups simultaneously.

The Trigger Flag bit is set as soon as an ADC channel meets the trigger criterion. This flag remains latched until the next event start, i.e. it will not be cleared as new ADC data which do not meet the trigger criterion come in with Wrap mode active.
The Trigger Flag Clear Counter register allows you to define a number of samples after which the Trigger Flag bit will be cleared unless a new trigger occurred. A counter (for the given ADC channel) is preloaded with the value of the Trigger Flag Clear counter register when the trigger criterion for this channel is met. Consecutive sampling clocks will decrement the counter and the Trigger Flag bit will be cleared as soon as the counter reaches 0. If a new trigger occurs before the counter has reached 0, it will be reloaded with the value from the register (retrigger).

Note: typically the user may want to set the value of the Trigger Flag Clear counter register to the memory page size, but this is not mandatory.

The Trigger Flag Clear Logic is disabled if the counter is loaded with 0 (power up default).

Bit	31-16	15-0
Function	unused, read back as 0	Trigger Flag Clear counter register

The power up default value is 0

4.22 Clock Predivider register *(0x100020, 0x200020, 0x280020, 0x300020, 0x380020)*

```
#define SIS3300_CLOCK_PREDIVIDER_ALL_ADC      0x100020  /* write only;D32 */

#define SIS3300_CLOCK_PREDIVIDER_ADC12        0x200020  /* read/write;D32 */
#define SIS3300_CLOCK_PREDIVIDER_ADC34        0x280020  /* read/write;D32 */
#define SIS3300_CLOCK_PREDIVIDER_ADC56        0x300020  /* read/write;D32 */
#define SIS3300_CLOCK_PREDIVIDER_ADC78        0x380020  /* read/write;D32 */
```

This register is implemented for each channel group and it has to be written with the same value. Use the address `SIS3300_CLOCK_PREDIVIDER_ALL_ADC` to write to the registers of all channel groups simultaneously.

The Clock Predivider factor (max. 255; 0xff) is defined by this register. It is used in multiplexer mode only.

Bit	Function	Default
31	Unused; read 0	0
..	..	
8	Unused; read 0	0
7	Clock Predivider bit 7 (MSB)	0
..	..	
0	Clock Predivider bit 0 (LSB)	0

The power up default value reads 0x 00000000

4.23 No_Of_Sample register (0x100024, 0x200024, 0x280024, 0x300024, 0x380024)

```
#define SIS3300_NO_OF_SAMPLE_ALL_ADC         0x100024  /* write only;D32 */

#define SIS3300_NO_OF_SAMPLE_ADC12           0x200024  /* read/write;D32 */
#define SIS3300_NO_OF_SAMPLE_ADC34           0x280024  /* read/write;D32 */
#define SIS3300_NO_OF_SAMPLE_ADC56           0x300024  /* read/write;D32 */
#define SIS3300_NO_OF_SAMPLE_ADC78           0x380024  /* read/write;D32 */
```

This register is implemented for each channel group and it has to be written with the same value.
Use the address `SIS3300_NO_OF_SAMPLE_ALL_ADC` to write to the registers of all channel groups simultaneously.

The No_of_Sample factor (max. 255; 0xff) is defined by this register. It is used in MULTIPEXER mode only.

Bit	Function	Default
31	Unused; read 0	0
..	..	
8	Unused; read 0	0
7	No_Of_Sample bit 7 (MSB)	0
..	..	
0	No_Of_Sample bit 0 (LSB)	0

The power up default value reads 0x 00000000

Note: The value of these registers (Clock Predivider , No_of_Sample) is copied autonomously to the 4 ADC groups. As the register is write only, the user will have to read back the value from one of the ADC groups in case read back functionality is desired.

4.24 Trigger setup register registers (0x100028, 0x200028, 0x280028, 0x300028, 0x380028)

```
#define SIS3300_TRIGGER_SETUP_ALL_ADC        0x100028  /* write only;D32 */

#define SIS3300_TRIGGER_SETUP_ADC12          0x200028  /* read/write;D32 */
#define SIS3300_TRIGGER_SETUP_ADC34          0x280028  /* read/write;D32 */
#define SIS3300_TRIGGER_SETUP_ADC56          0x300028  /* read/write;D32 */
#define SIS3300_TRIGGER_SETUP_ADC78          0x380028  /* read/write;D32 */
```

This bit register is implemented on the channel group, the register `SIS3300_TRIGGER_SETUP_ALL_ADC` is used to write to the registers of all channel groups simultaneously.
The behaviour of the trigger output of the SIS3300 can be controlled by this register. The user can select between a N over, M under threshold or a pulsed trigger output with pulse width P. At the same time the register holds the values for N, M and P as shown in the table below.

Bit	
31	reserved; read 0
30	reserved; read 0
29	reserved; read 0
28	enable pulse mode
27	reserved; read 0
26	reserved; read 0
25	reserved; read 0
24	enable N M mode
23	reserved; read 0
...	...
20	reserved; read 0
19	bit 3 of P
18	bit 2 of P
17	bit 1 of P
16	bit 0 of P
15	reserved; read 0
...	...
12	reserved; read 0
11	bit 3 of N
10	bit 2 of N
9	bit 1 of N
8	bit 0 of N
7	reserved; read 0
...	...
4	reserved; read 0
3	bit 3 of M
2	bit 2 of M
1	bit 1 of M
0	bit 0 of M

The power up default value reads 0x 00000000

4.25 MAX No of Events registers (0x10002C, 0x20002C, 0x28002C, 0x30002C, 0x38002C)

```
#define SIS3300_MAX_NO_OF_EVENTS_ALL_ADC      0x10002C  /* write only;D32 */

#define SIS3300_ MAX_NO_OF_EVENTS_ADC12       0x20002C  /* read/write;D32 */
#define SIS3300_ MAX_NO_OF_EVENTS_ADC34       0x28002C  /* read/write;D32 */
#define SIS3300_ MAX_NO_OF_EVENTS_ADC56       0x30002C  /* read/write;D32 */
#define SIS3300_ MAX_NO_OF_EVENTS_ADC78       0x38002C  /* read/write;D32 */
```

This register is implemented for each channel group and it has to be configured to the same value in all groups, what is done most straightforward by writing to the address `SIS3300_MAX_NO_OF_EVENTS_ALL_ADC`.

This register is used in GATE Chaining / Multi Event Mode only.
It limits the number of Events in the GATE Chaining / Multi Event Mode.

ate chaining mode sampling will stop when
a.) the maximum number of events is reached or
b.) the end of bank is reached. In this case the last event/gate may be incomplete.

Bit	31-16	15-0
Function	unused, read back as 0	Max_No_Of_Events

The power up default value is 0

4.26 Trigger event directory bank 1 (0x101000 – 0x101ffc)

```
#define SIS3300_EVENT_DIRECTORY_BANK1_ALL_ADC  0x101000
                                    /* read only; D32, BLT32; size: 0x1000 */
```

This Trigger event directory holds the stop pointer(s) (i.e. end address+1) of memory bank 1. The directory is 32 bits wide, a wrap around bit (i.e. bit 19) will be set if the page was filled at least once (i.e. if the memory pointer has reached the end)

offset address	(D31)	(D30)	(D29)	(D28)	(D27)	(D26)	(D25)	(D24)	(D21:20)	(D19)	(D18:D17)	Event Data End Address (D16:D0)
0x0	T1	T2	T3	T4	T5	T6	T7	T8	0	W	0	(End Address + 1) of Event 0
..	...	...	...	...	...	...	...	...	...	...		...
0xffc	T1	T2	T3	T4	T5	T6	T7	T8	0	W	0	(End Address + 1) of Event 1023

W: wrap around bit
T1-T8 trigger information ADC 1 - ADC 8,
1: ADC channel has met trigger criterion for this event
0: ADC channel has not triggered for this event

4.27 Trigger event directory bank 2 (0x102000 – 0x102ffc)

```
#define SIS3300_EVENT_DIRECTORY_BANK2_ALL_ADC  0x102000
                                    /* read only; D32, BLT32; size: 0x1000 */
```

Same as above, but for bank 2.

4.28 Event directories bank 1 *(0x201000 – 0x201ffc, 0x281000 – 0x281ffc, 0x301000 – 0x301ffc, 0x381000 – 0x381ffc)*

```
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC12     0x201000
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC34     0x281000
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC56     0x301000
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC78     0x381000
                                  /* read only; D32, BLT32; size: 0x1000 */
```

These arrays are redundant and not used in standard operation, use the trigger event directory instead.
The event directories hold the stop pointer(s) (i.e. end address+1) of each channel group of memory bank 1.
The directories are 32 bits wide, a wrap around bit (i.e. bit 19) will be set if the page was filled at least once (i.e. if the memory pointer has reached the end)

offset address	(D31:24)	(D23:22)	(D21:20)	(D19)	(D18:D17)	Event Data End Address (D16:D0)
0x0	0	T2, T1	0	W	0	(End Address + 1) of Event 0
..	...	...	...	...		...
0xffc	0	T2, T1	0	W	0	(End Address + 1) of Event 1023

W: wrap around bit
T1, T2 trigger information ADC 1/3/5/7 , ADC 2/4/6/8 of channel group

4.29 Event directories bank 2 *(0x202000 – 0x202ffc, 0x282000 – 0x282ffc, 0x302000 – 0x302ffc, 0x382000 – 0x382ffc)*

```
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC12     0x202000
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC34     0x282000
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC56     0x302000
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC78     0x382000
                                  /* read only; D32, BLT32; size: 0x1000 */
```

Same as above, but for bank 2.

4.30 Bank 1 address counter (0x200008, 0x280008, 0x300008, 0x380008)

```
#define SIS3300_BANK1_ADDR_CNT_ADC12        0x200008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC34        0x280008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC56        0x300008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC78        0x380008   /* read only;D32 */
```

These read only registers hold the current bank 1 address counter for ADC group 1/2/3/4 and bank. The counter is 17 –bit wide. The counter will change while the ADC is sampling, after the ADC was stopped, the stop position can be retrieved (in multi event mode it will have to be read from the event directory). The address counter points to the next memory location that will be written to (see Trigger event directory also).

The register is implemented on the channel group base, but the information is redundant and in the standard readout case you will want to retrieve the information from one channel group only.

Bit	31-17	16-0(*)
Function	unused, read back as 0	address counter

The address counter is not in a defined state after power up or Key Reset

(*) Unused bits are not updated and may contain arbitrary data, i.e. only the number of bits that corresponds to the selected page size will hold significant data (example: the lowest 7 bits are valid for a page size of 128).

4.31 Bank 2 address counter (0x20000C, 0x28000C, 0x30000C, 0x38000C)

```
#define SIS3300_BANK2_ADDR_CNT_ADC12        0x20000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC34        0x28000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC56        0x30000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC78        0x38000C   /* read only;D32 */
```

Same as bank 1 address counters, but for bank 2 of ADC groups 1/2/3/4.

4.32 Bank 1 event counter (0x200010, 0x280010, 0x300010, 0x380010)

```
#define SIS3300_BANK1_EVENT_CNT_ADC12       0x200010   /* read only;D32 */
#define SIS3300_BANK1_EVENT_CNT_ADC34       0x280010   /* read only;D32 */
#define SIS3300_BANK1_EVENT_CNT_ADC56       0x300010   /* read only;D32 */
#define SIS3300_BANK1_EVENT_CNT_ADC78       0x380010   /* read only;D32 */
```

This read only registers hold the current bank 1 event counter for ADC groups 1/2/3/4. The counter is 12–bit wide. The counter will change while the ADC is sampling (as events are coming in). The returned value is the current event number.

The register is implemented on the channel group base, but the information is redundant and in the standard readout case you will want to retrieve the information from one channel group only.

Bit	31-16	15-0
Function	unused, read back as 0	event counter

The event counter is not in a defined state after power up or Key Reset

4.33 Bank 2 event counter (0x200014, 0x280014, 0x300014, 0x380014)

```
#define SIS3300_BANK2_EVENT_CNT_ADC12       0x200014   /* read only;D32 */
#define SIS3300_BANK2_EVENT_CNT_ADC34       0x280014   /* read only;D32 */
#define SIS3300_BANK2_EVENT_CNT_ADC56       0x300014   /* read only;D32 */
#define SIS3300_BANK2_EVENT_CNT_ADC78       0x380014   /* read only;D32 */
```

Same as bank 1 event counter, but for bank 2 of ADC groups 1-4.

4.34 Actual Sample registers (0x200018, 0x280018, 0x300018, 0x380018)

```
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC12   0x200018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC34   0x280018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC56   0x300018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC78   0x380018   /* read only;D32 */
```

Read “on the fly” of the actual converted ADC values.
The registers are updated with every ADC clock, unless a concurrent VME read access is pending.
The register contents is refreshed and can be read any time (i.e. they are updated independent of the unarmed, armed, sampling state) as long as a sampling clock is distributed on the ADC board (internal clock or active/clocking external clock)

For SIS3300:

ADC 1 / 3 / 5 / 7			ADC 2 / 4 / 6 / 8		
D31:29	D28	D27:16	D15:13	D12	D11:0
0 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data

For SIS3301:

ADC 1 / 3 / 5 / 7			ADC 2 / 4 / 6 / 8		
D31	D30	D29:16	D15	D14	D13:0
0	OR bit	14-bit data	0	OR bit	14-bit data

OR : Out of range, set with over or underflow

4.35 Bank 1 memory (0x400000 – 0x5ffffc)

```
#define SIS3300_MEMBASE_BANK1_ADC12             0x400000
#define SIS3300_MEMBASE_BANK1_ADC34             0x480000
#define SIS3300_MEMBASE_BANK1_ADC56             0x500000
#define SIS3300_MEMBASE_BANK1_ADC78             0x580000
        /* write D32; read D32, BLT32, MBL64, 2eVME; size: 0x80000 */
```

Bank1 memory is divided into 4 channel groups of 128 KSamples each (i.e. 512 KByte deep for every channel group, 2MByte in total). The 32-bit wide memory locations hold the data of 2 ADCs each. Readout can be done with D32, BLT32, MBLT64 or 2eVME, for memory tests D32 write cycles only are supported.

Notes:

- “FIFO” block transfer cycles (i.e. readout from a constant VME address in block transfer) are supported from every channel group (internal 17-bit address counter, A18 to A2)
- 2eVME cycles have to start on a 0x100 boundary (0x0, 0x100, 0x200 ...)

Data format for SIS3300:

offset address	ADC 1 / 3 / 5 / 7				ADC 2 / 4 / 6 / 8			
	D31	D30:29	D28	D27:16	D15	D14:13	D12	D11:0
0x0	U	0 0	OR bit	12-bit data	G	0 0	OR bit	12-bit data
..								
0x7fffc	U	0 0	OR bit	12-bit data	G	0 0	OR bit	12-bit data

Data format for SIS3301:

offset address	ADC 1 / 3 / 5 / 7			ADC 2 / 4 / 6 / 8		
	D31	D30	D29:16	D15	D14	D13:0
0x0	U	OR bit	14-bit data	G	OR bit	14-bit data
..						
0x7fffc	U	OR bit	14-bit data	G	OR bit	14-bit data

Shorthand	Explanation
U	status of user bit if enabled, 0 otherwise
OR	out of range, set with over or underflow, 0 otherwise
G	set on the first sample in “Gate Chaining Mode”, 0 otherwise

4.36 Bank 2 memory (0x600000 – 0x7ffffc)

```
#define SIS3300_MEMBASE_BANK2_ADC12             0x600000
#define SIS3300_MEMBASE_BANK2_ADC34             0x680000
#define SIS3300_MEMBASE_BANK2_ADC56             0x700000
#define SIS3300_MEMBASE_BANK2_ADC78             0x780000
```

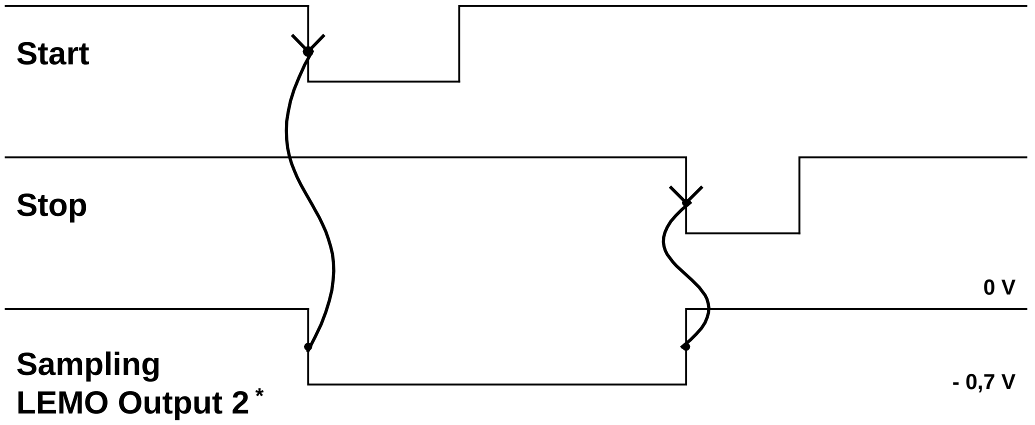
Bank 2 memory is installed to allow for parallel readout from one memory bank, while the other memory bank is acquiring data. The second memory bank has the same structure as bank 1.

5 Description of Start/Stop and Gate operation modi

5.1 Start/stop mode

Different start and stop conditions can be used in combination with start/stop mode (as illustrated in the start and stop logic summaries.

Note: * LEMO output 2 (ready for stop) reflects the phase in which the digitizer is sampling, unless the signal was assigned to reflect the bank full pulse (by setting bit 9 of the control register)



5.1.1 Front panel start/stop

One option to use start stop/mode is with NIM front panel start and stop signals. The width of the start and stop pulse has to exceed 2 sampling clocks. Following steps are part of the setup in this case.

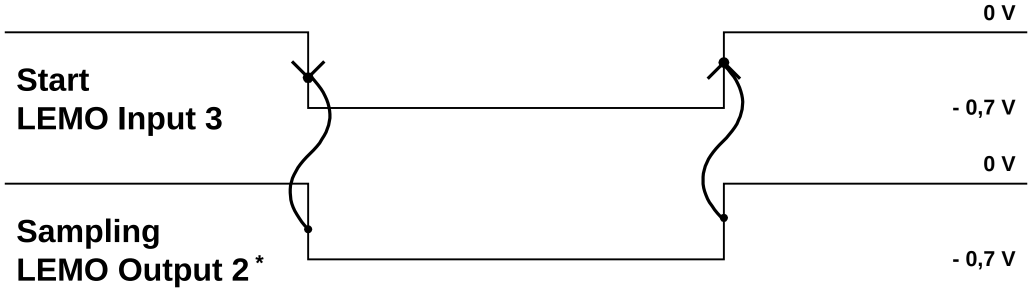
- enable front panel start/stop logic (by setting bit 8 of acquisition control register)
- connect start to LEMO input 3
- connect stop to LEMO input 2

5.2 Gate mode

A single external signal is used to define sampling start and stop. The start signal (i.e. LEMO input 3) is used as gate input in this mode. The leading edge of the signal defines the start, the stop condition is given by the trailing edge as illustrated below. The width of the gate has to exceed 2 sample clocks.

Following steps are required to activate gate mode

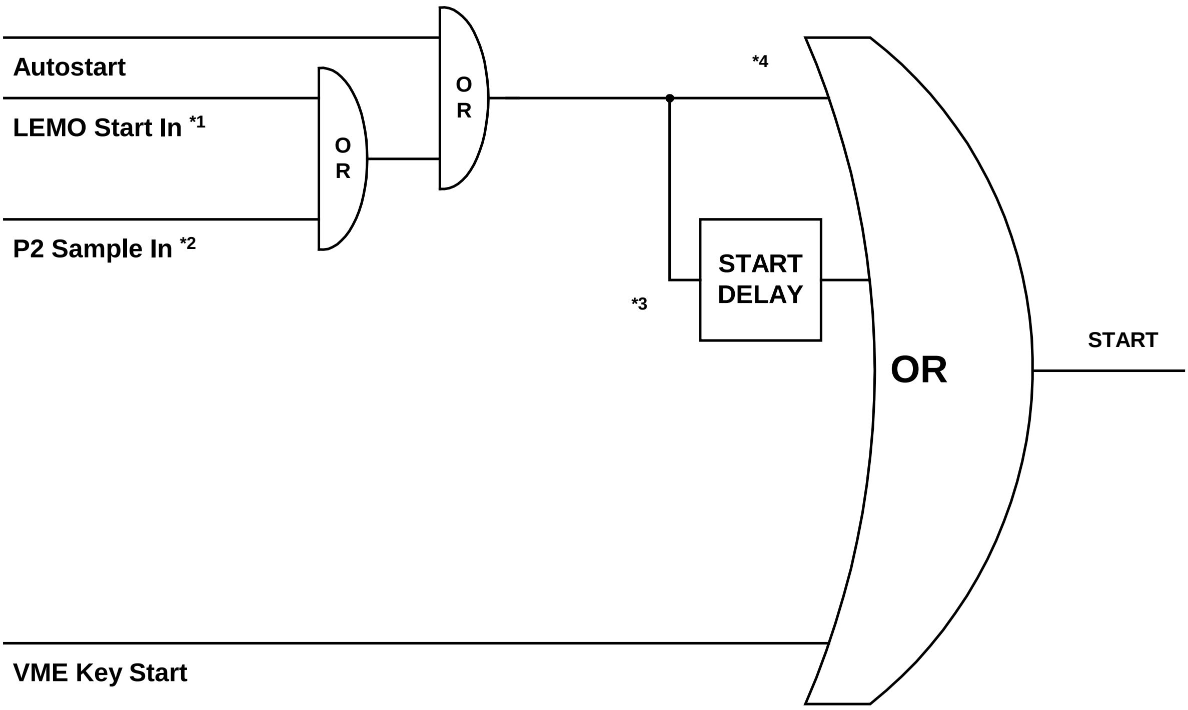
- enable front panel start/stop logic (set bit 8 of acquisition control register)
- enable front panel gate mode (set bit 10 of acquisition control register)



Note: * LEMO output 2 (ready for stop) reflects the phase in which the digitizer is sampling, unless the signal was assigned to reflect the bank full pulse (by setting bit 9 of the control register)

5.3 Start logic summary

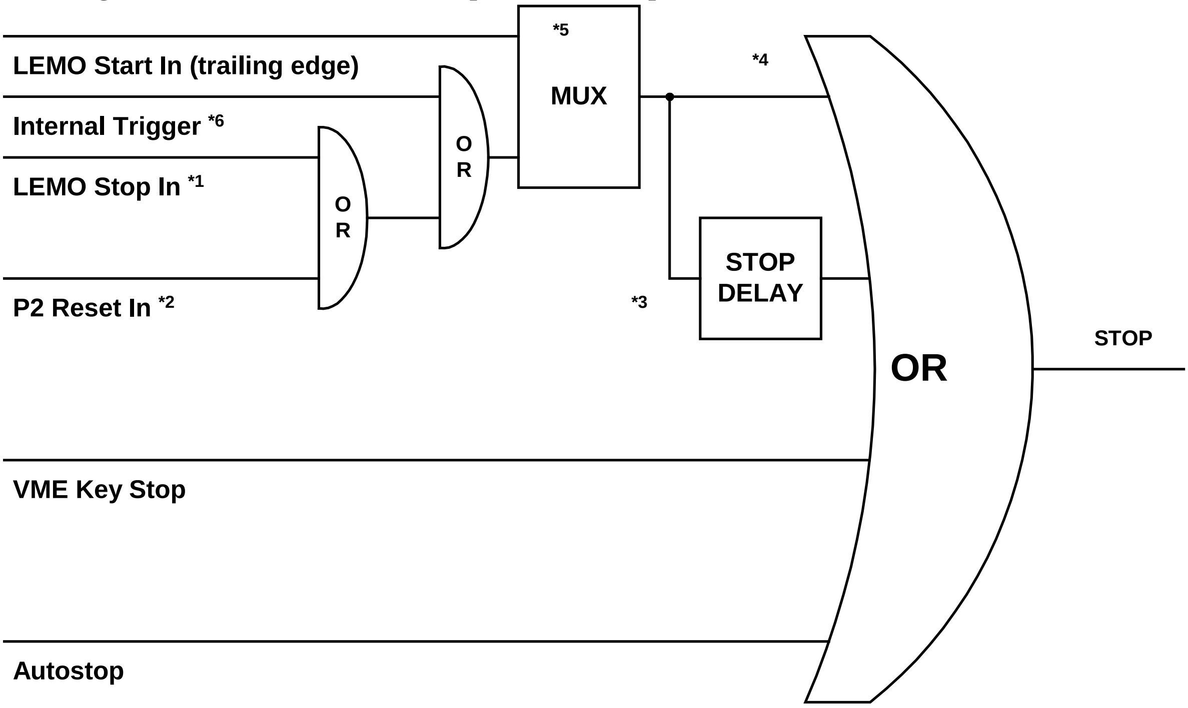
The diagram below illustrates the implemented start conditions of the SIS3300/1,



Note	Condition	Register	Comment
*1	`Bit 8 = 1`	Acquisition Control	Enable front panel start/stop logic
*2	`Bit 9 = 1`	Acquisition Control	Enable P2 start/stop logic
*3	`Bit 6 = 1`	Acquisition Control	Start delay enable
*4	`Bit 6 = 0`	Acquisition Control	No start delay

5.4 Stop logic summary

The diagram below illustrates the implemented stop conditions of the SIS3300/1,



Note	Condition	Register	Comment
*1	`Bit  8 = 1`	Acquisition Control	Enable front panel start/stop logic
*2	`Bit  9 = 1`	Acquisition Control	Enable P2 start/stop logic
*3	`Bit  7 = 1`	Acquisition Control	Stop delay enable
*4	`Bit  7 = 0`	Acquisition Control	No stop delay
*5	`Bit 10 = 0` `Bit 10 = 1`	Acquisition Control	use start/stop mode use gate mode
*6	`Bit  6 = 1`	Control	Route trigger

6 Operation

6.1 Configuration:

- Issue key reset

- define in Interrupt configuration register
  - VME IRQ Level and Vector
  - type of IRQ requester

- define in Interrupt control register
  - enable IRQ source

- define in Acquistion register
  - Set Clock source
  - Set Start/Stop or Gate mode
  - Enable/Disable P2 External Start/Stop
  - Enable/Disable LEMO External Start/Stop
  - Enable/Disable External Stop Delay
  - Enable/Disable External Start Delay
  - Set Single or Multi Event Mode
  - if Multi Event then enable/disable Autostart

- define in Event configuration register
  - Enable/Disable Autostop at end address of Page
  - Set Page size

6.2 Arm for sampling:

- define in Acquistion register
  - Enable Sample Clock for Memory Bank1 or Bank2

6.3 Start Sampling:

- in Single Event mode
  - Issue key Start or External Start

- in Multi Event mode with Autostart disabled
  - Issue key Start or External Start for **each** Event

- in Multi Event mode with Autostart enabled
  - Issue key Start or External Start for the **first** Event only

Note: activation of auto bank switch mode with multi event mode enabled will start sampling automatically

6.4 Stop Sampling (Event):

- in Single Event mode with Autostop enabled
  - sampling stops automatically at the end address of the page

- in Single Event mode with Autostop is disabled (Wrap around mode)
  - Issue key Stop or External Stop

- in Multi Event mode with Autostop is enabled
  - sampling stops automatically at the end address of each page

- in Multi Event mode with Autostop is disabled (Wrap around mode)
  - Issue key Stop or External Stop for each Event

6.5 End of Sampling (clear arm / disable Sample Clock):

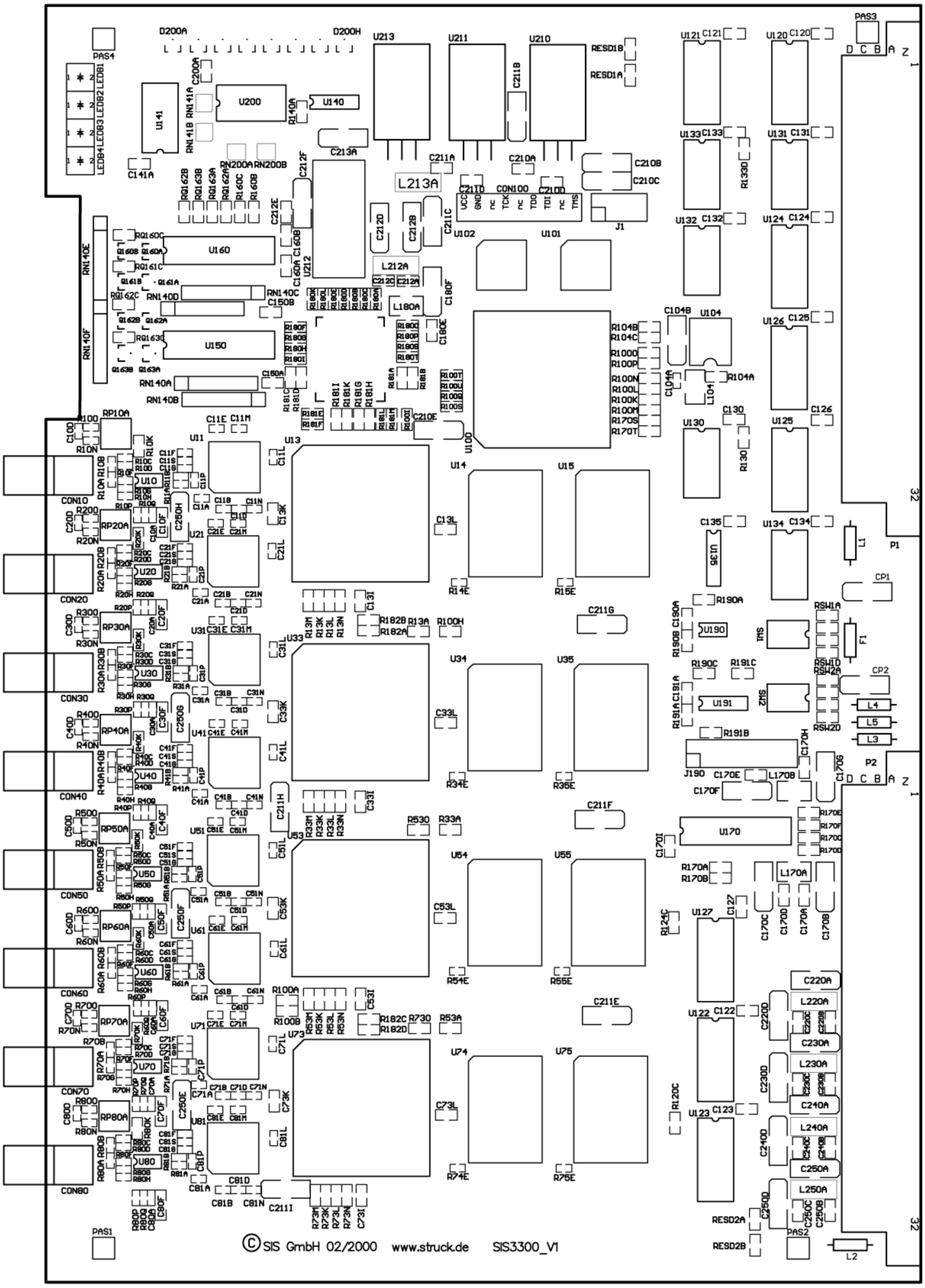
- in single event mode
  the "Sample Clock Enable " bit of the sampling bank is cleared by the logic at the end of sampling (one event)

- in multi event mode
  the "Sample Clock Enable " bit of the sampling bank is cleared by the logic at the end of sampling (last event)

The user software can poll on the status of the sample clock enable bit in the acquisition control register or use the end of event or bank full interrupt conditions.

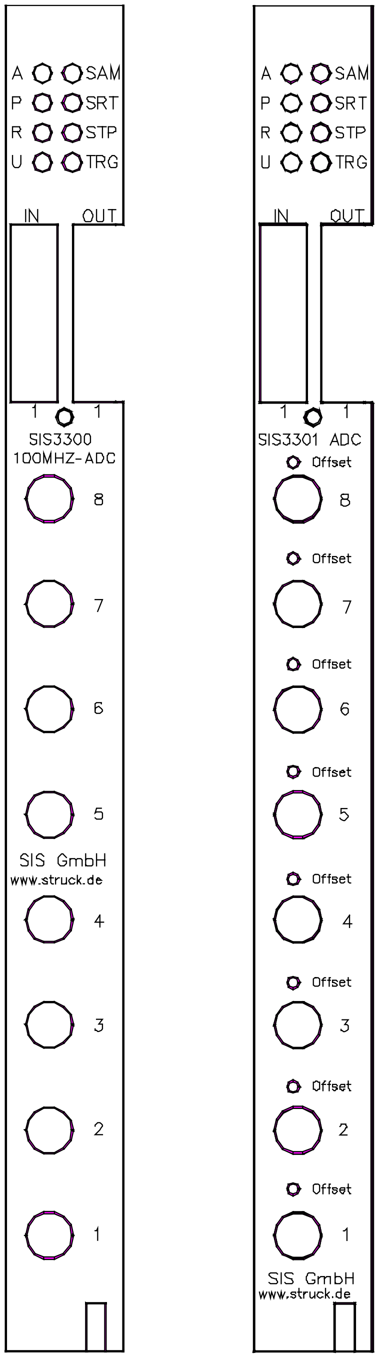
7 Board layout

A printout of the silk screen of the component side of the PCB is shown below.



8 Front panel

The SIS3300 is a single width (4TE) 6U VME module. A sketch of the SIS3300 (left hand side) and SIS3301 front panels (without handles) is shown below.



8.1 Control In/Outputs

The control I/O section features 8 LEMO00 connectors with NIM levels.

Designation	Inputs	Outputs	Designation
4	Clock In	Clock Out	4
3	Start	Ready for Start/bank full output	3
2	Stop	Ready for Stop/bank full output	2
1	User in	User out/trigger/Multiplexer Strobe/bank full output	1

The ready for start and ready for stop outputs can be used to interfere with external deadtime logic. Ready for start will become active as soon as the sample clock for one of the banks is active. Ready for stop will go active as soon as the start signal was seen by the module.

The external clock must be a symmetric signal unless the module is operated in external random clock mode
The width of an external start/stop pulse must be greater or equal two sampling clock periods.

8.1.1 User input

User input functionality was implemented to allow for synchronous recording of one external status bit (like chopper on/off e.g.) with the ADC data stream. The user bin information is recorded with the ADC data (see section 4.35). The current status of the logic level is represented by Bit 16 of the status register.

8.1.2 Control input termination

The control inputs are configured for 50 Ω termination (i.e. with 47 Ω) by default.
Each input is terminated with a resistor network (5 pins, 4 resistors, common pin to socket pin 6) to ground, the names of the input sockets are listed in the table below.

Designation	Inputs	Resistor Network
4	Clock In	RN140A
3	Start	RN140B
2	Stop	RN140C
1	User in	RN140D

8.2 Analog inputs

8.2.1 Input range and impedance configuration for single ended SIS3300/1

Input impedance and range are configured with a set of SMD resistors. The input range configuration is a combination of selecting the requried input voltage span and a possible input shift by means of a potentiometer. A unit with an input range of +2.5 V ... –2.5 V and a module with 0 V ... –5 V both have a span of 5 V, which is shifted by -2.5 V to the negative side in the later case e.g.

The table below lists the configuration for ADC channel 1. The other channels are configured with their corresponding resistors (R20A, ..., R20I for channel 7 e.g.).

Voltage span	Impedance	R10A	R10B	R10D	R10E	R10F	R10G	R10H	R10I
1 V	50 Ohm	50	0	560	1.2k	25	0	560	1.2k
2 V	50 Ohm	50	0	560	560	25	0	560	560
2 V	1 Kohm	1.2K	0	1.2k	1.2k	25	0	1.2k	1.2k
3 V	50 Ohm	50	680	33	511	25	680	33	511
4 V	50 Ohm	50	1k	15	560	25	1k	15	560
5 V	50 Ohm	50	1.2k	15	560	25	1.2k	15	560
8 V	75 Ohm	75	2k	0	560	33	2k	0	560

Note: defects that are due to in field input range configuration change are not covered by the modules warranty

8.2.2 Input range and impedance for differential SIS3301

The differential version of the SIS3301 has an input impedance of 100 Ohms and an input range of +1 V ... –1V.

8.3 LED's

The SIS3300 has 8 front panel LEDs to visualise part of the modules status. The user (and access) LED are a good way to check first time communication/addressing with the module.

Color	Designator	Function
Red	A	Access to SIS3300 VME slave port
Yellow	P	Power
Green	R	Ready, on board logic configured
Green	U	User, to be set/cleared under program control
Red	SAM	Sampling,
Yellow	SRT	Start, lit with start input (or leading edge in gate mode)
Green	STP	Stop, lit with stop input (or trailing edge in gate mode)
Green	TRG	Trigger, lit if one or more channels are above threshold

The on duration of the access, sampling, start, stop and trigger LEDs is stretched to guarantee visibility even under low rate conditions.

8.4 PCB LEDs

The 8 surface mounted red LEDs D200A to D200H on the top left corner of the component side of the SIS3300 are routed to the control FPGA, their use may depend on the firmware design.

9 Jumpers/Configuration

9.1 J1

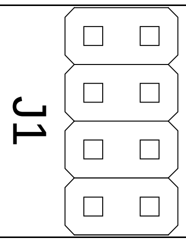
The function of J1 depends on the PCB (printed circuit board) revision level. The board revision level is printed in white on the lower edge of the card on the component side as a text of the form SIS3300_V1 e.g.

9.1.1 SIS3300_V1

Selection of bits 31-28 of the 32-bit A32 address (see. base address section)

9.1.2 SIS3300_V2 (and higher)

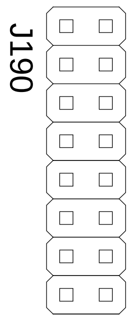
The SIS3300 supports several addressing modes, the actual mode is selected by jumper array J1. The given mode is selected if its corresponding jumper is in place. The four jumper positions are described in the table below. The A32 jumper is closest to the modules front panel.



Jumper	Function	Factory default
A32	enable A32 addressing	closed
GEO	enable geographical addressing	open
VIPA	not implemented yet	open
reserved	reserved	open

9.2 J190 Reset

Jumper 5 of jumper array J190 defines the reset behaviour of the SIS3300 upon VME Sysreset. If the jumper is closed the module will be reset with VME Sysreset. The other fields of the array are unused in the current firmware design.



Jumper	Function	Factory default
1	unused	open
2	enable watchdog	closed
3	unused	open
4	unused	open
5	unused	open
6	Connect module reset to VME_Sysreset	closed
7	unused	open
8	unused	open

The enable watchdog jumper has to be removed during the initial JTAG firmware load.

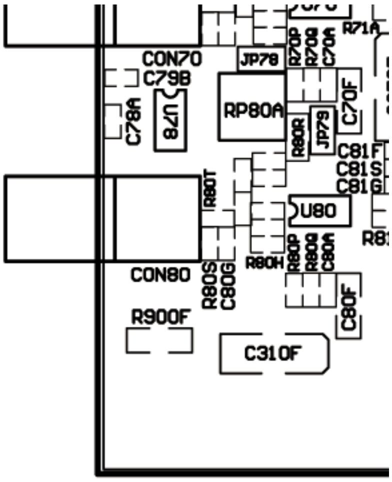
9.3 Offset adjustment

9.3.1 SIS3300

The pedestal or offset of single ended (non symmetric) ADC channels can be adjusted with the potentiometers RP10A through RP80A (see table below). The sensitivity for the positive or negative offset can be reduced by two limit jumpers (2 mm), the full range is available with both jumpers open. Do not install both jumpers for a channel in parallel.

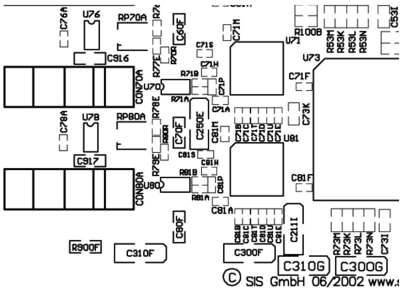
channel	limit pos. offset	limit neg. offset	Offset-Potentiometer
1	JP78	JP79	RP80A
2	JP76	JP77	RP70A
3	JP58	JP59	RP60A
4	JP56	JP57	RP50A
5	JP38	JP39	RP40A
6	JP36	JP37	RP30A
7	JP18	JP19	RP20A
8	JP16	JP17	RP10A

The position of the two jumpers JP78 and JP79 close to potentiometer RP80A for ADC channel 1 is illustrated in the portion of the board shown below. The displayed area is the vicinity of the channel 1 LEMO input connector (CON80).



9.3.2 SIS3301

Due to the higher sensitivity of the 14-bit ADC it is expected, that this design will be mainly used with differential and/or symmetric inputs. Potentiometers can be installed, but the limit jumpers are not present in the design.



9.4 JTAG

The SIS3300 on board logic can load its firmware either from two serial PROMs or via the JTAG port on connector CON100. A list of firmware designs can be found under http://www.struck.de/sis3300firm.htm.

Hardware like the XILINX HW-JTAG-PC in connection with the appropriate software will be required for in field JTAG firmware upgrades.

The JTAG connector is a 9 pin single row 1/10 inch header, the pin assignment on the connector can be found in the table below.

Pin	Short hand	Description
1	VCC	Supply voltage
2	GND	Ground
3	nc	not connected, cut to avoid polarity mismatch
4	TCK	test clock
5	nc	not connected
6	TDO	test data out
7	TDI	test data in
8	nc	not connected
9	TMS	test modus

10 Appendix

10.1 Data acquisition modes

10.1.1 Multiplexer mode

Multiplexer mode was implemented to facilitate data acquisition with external multiplexing hardware. One of the outputs of the SIS3300 can be used to control the external multiplexing circuitry.
Multiplexer mode is activated by setting Bit 15 of the acquisition control register. Upon a start (external or via VME key address) the analog input will be latched to memory after (N –10) * clock cycles. At the same time a pulse of width one clock cycle will be generated on ouput 1. Acquisition will terminate after M samples.

* The ADC has an internal pipeline of 12 Clock cycles.
Note: The minimum value for the Predivider register value is 4

Example : Assume one multiplexing cycle consists of 20 words. The analog signal will become valid after 11 µs and will be written to memory after 12 µs.

Set internal Sampling clock to 12.5 MHz Clock cycle = 80 ns
Preset Predivider register to 0x96 (150) 150 x 80 ns = 12 µs
Preset No_Of_Sample register to 0x14 (20)
Write 0x8000 (set Bit 15) to acquisition control register.

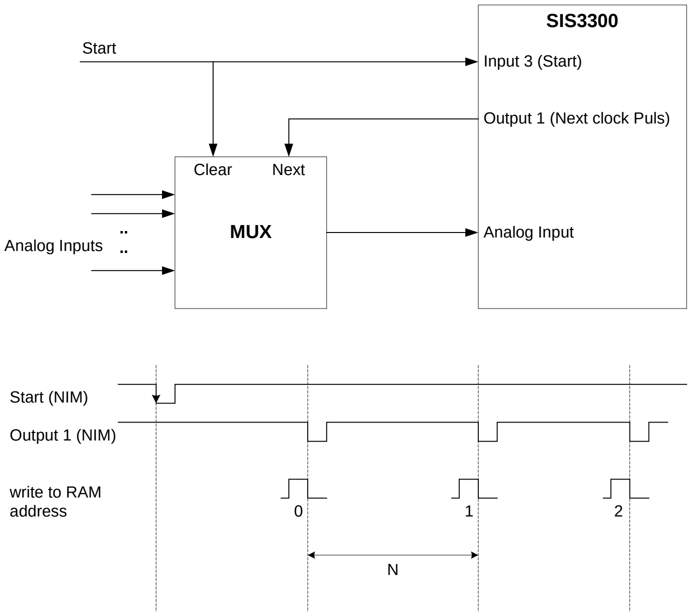


Illustration of multiplexer mode

10.1.2 Random external clock mode

The minimum clock frequency of the analog to digital converter chips of the SIS3300 and 3301 is limited. Random external clock mode was implemented to allow to acquire data at arbitrary low clock frequencies and irregular clock. The digitizer will sample at the selected internal clock speed (50 MHz e.g.), but no data are stored to memory until an external clock pulse is detected. The internal clock will strobe a datum to memory upon recognition of a leading edge on the clock input.
Random external clock mode is activated by writing 0x800 to the acquisition control register .

10.1.3 *wrap versus single shot/no wrap mode*

The SIS330x can be operated in single shot (no wrap) or wrap mode in both single and multi event mode.

10.1.3.1 single shot

The digitizer will acquire data until the end of event once it is started. The first datum is at the beginning of the event, the last datum is stored at the end of the event.

10.1.3.2 wrap mode

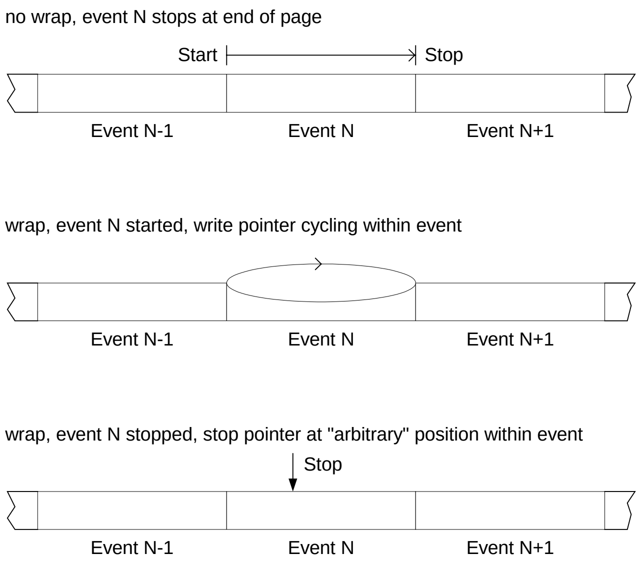
The digitizer will acquire data until it is stopped by one of the stop conditions. At the end of event the memory write pointer will wrap to the beginning of the event and old data are overwritten by the latest digitized values. The memory/stop pointer can be at any position within the event after the stop and the data set has to be rearranged after readout to have it in one consecutive block. You will have to check the wrap bit in the event directory upon readout to know, whether the data from stop pointer to the end of event are valid also (what is the case as soon as the memory pointer has wrapped once. The first part of the event sits between stop pointer and end of event if the wrap bit had been set and the second portion sits from the start of event until the stop pointer. If the stop delay is active the stop delay will run down before the digitizer will actually stop to acquire data and this functionality can be used to have both data from before and after the stop in memory.

Example:

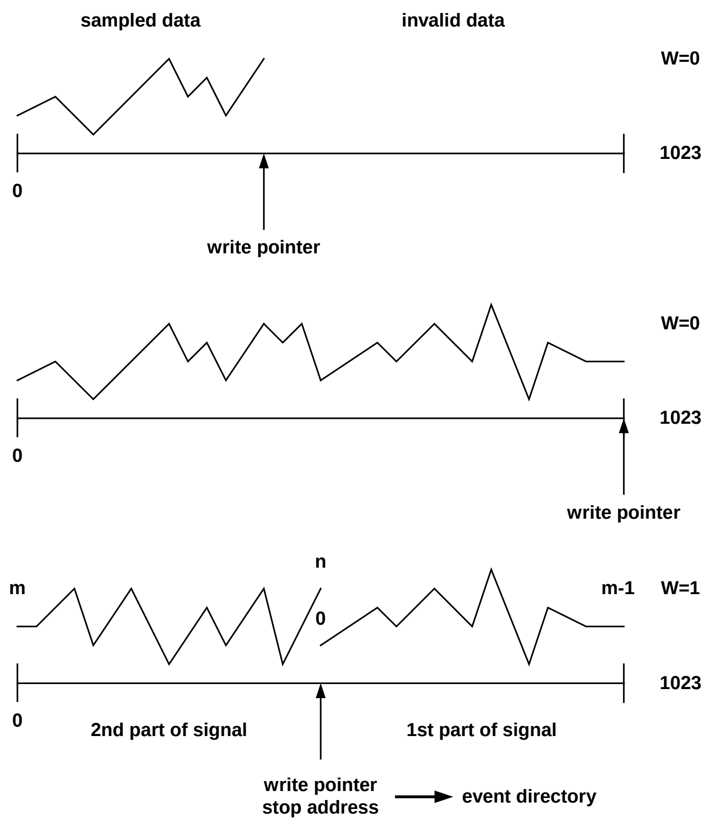
- multi event mode
- event size 1024 (i.e. 128 events per bank)
- stop delay 512

The digitizer will have 512 samples pre- and 512 samples post trigger recorded. After rearrangement of the data (see above) the location of the stop will be in the middle of the array.

Wrap mode will be used in conjunction with multi event and auto start mode in most cases, to start the digitizer with minimum delay after an event has been acquired.



The memory write pointer will increment with the ADCs clock and the digitized values are stored to the addressed memory location. The wrap bit will be set (W=1) in the event and trigger event directory for the given event if the pointer has wrapped around at least once. In that case the event is split as illustrated in the lowest trace below. If the wrap bit is not set (W=0), the entries from the beginning of the event/page up the the stop pointer are valid only. The rest of the page/event may hold arbitrary data from earlier acquisition cycles in that case.



10.1.4 Auto bank switch mode

Auto bank switch mode was introduced for efficient use of the two memory banks on acquisition . The mode is activated by issuing a KEY_START_AUTO_BANK_SWITCH after the feature was activated by setting bit 2 in the acquisition control register. The bank full flags (B1_FULL and B2_FULL) are cleared with the KEY, at the same time a first start is generated if AUTOSTART is enabled also. Data will be acquired into memory bank 1 until the bank is full. At this point the flag B1_FULL will be set and acquisition changes over to bank 2 (if the flag B2_FULL is not set). The user can read out data from bank 1 in parallel to ongoing acquisition into bank 2 and clear the B1_FULL flag after the readout was completed. As soon as memory bank 2 is filled acquisition will be handed over to bank 1 again if B1_FULL has been cleared already.
The active memory bank will acquire data until the bank is filled if a KEY-STOP_AUTO_BANK_SWITCH is issued.

10.2 Power consumption

The SIS3300/1 is a single supply design to facilitate operation in any VME environment, i.e. the module does not require special backplanes or non standard VME voltages.
The power consumption of a two memory bank module digitizing at 100 MHz was measured to be:

Voltage	Current
+ 5V	< 6A
+12 V	< 40 mA
- 12 V	< 60 mA
P < 32 W	

10.3 Operating conditions

10.3.1 Cooling

Although the SIS3300/1 is mainly a 2.5 and 3.3 V low power design, substantial power is consumed by the Analog to Digital converter chips and linear regulators. Hence forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at an ambient temperature between 10° and 40° Celsius. A power up warm up time of some 10 minutes is recommended to ensure equilibrium on board temperature conditions.

10.3.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3300 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

10.4 Connector types

The VME connectors and the two different types of front panel connectors used on the SIS3300 are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
LEMO PCB	Coax. control connector	LEMO EPB.00.250.NTN
90^o PCB LEMO	Analog input connector	LEMO EPL.00.250.NTN
90^o PCB LEMO	Analog input connector (3301 differential input version)	LEMO EPG.00.302.NLN

10.5 P2 row A/C pin assignments

The P2 connector of the SIS3300 has several connections on rows A and C for the F1002 compatible use at the DESY H1 FNC subdetector. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3300 is shown below:

P2A	Function	P2C	Function
1	-5.2 V	1	-5.2 V
2	-5.2 V	2	-5.2 V
3	-5.2 V	3	-5.2 V
4	not connected	4	not connected
5	not connected	5	not connected
6	DGND	6	DGND
7	P2_CLOCK_H	7	P2_CLOCK_L
8	DGND	8	DGND
9	P2_START_H	9	P2_START_L
10	P2_STOP_H	10	P2_STOP_L
11	P2_TEST_H	11	P2_TEST_L
12	DGND	12	DGND
13	DGND	13	DGND
14	DGND	14	DGND
15	DGND	15	DGND
16	not connected	16	not connected
...	...	17	...
31	not connected	18	not connected

Note: The P2 ECL signals are bussed and terminated on the backplane of F1002 crates. The user has to insure proper termination if a cable backplane or add on backplane is used.

10.6 Row d and z Pin Assignments

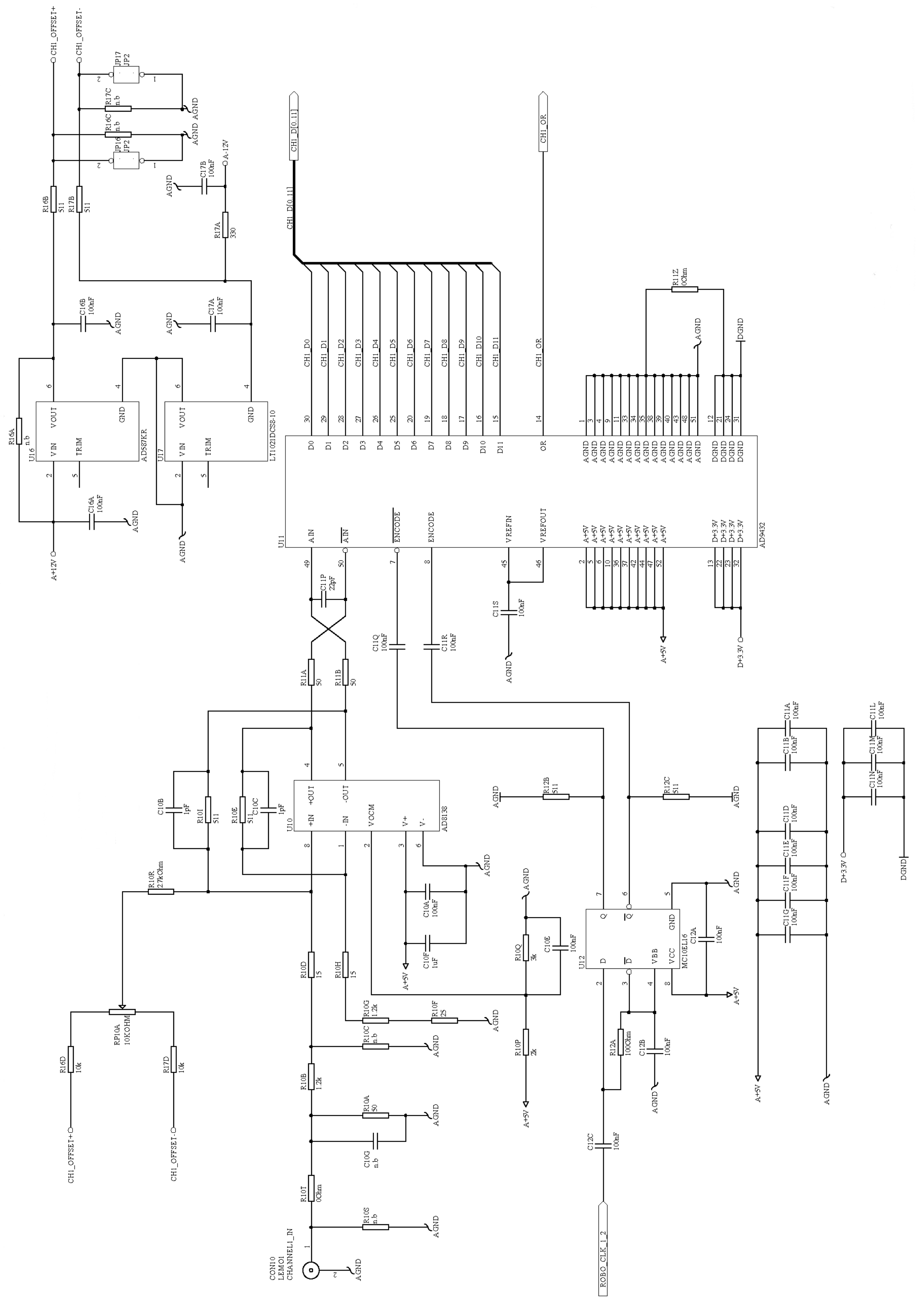
The SIS3300 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing (PCB revisions V2 and higher) and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

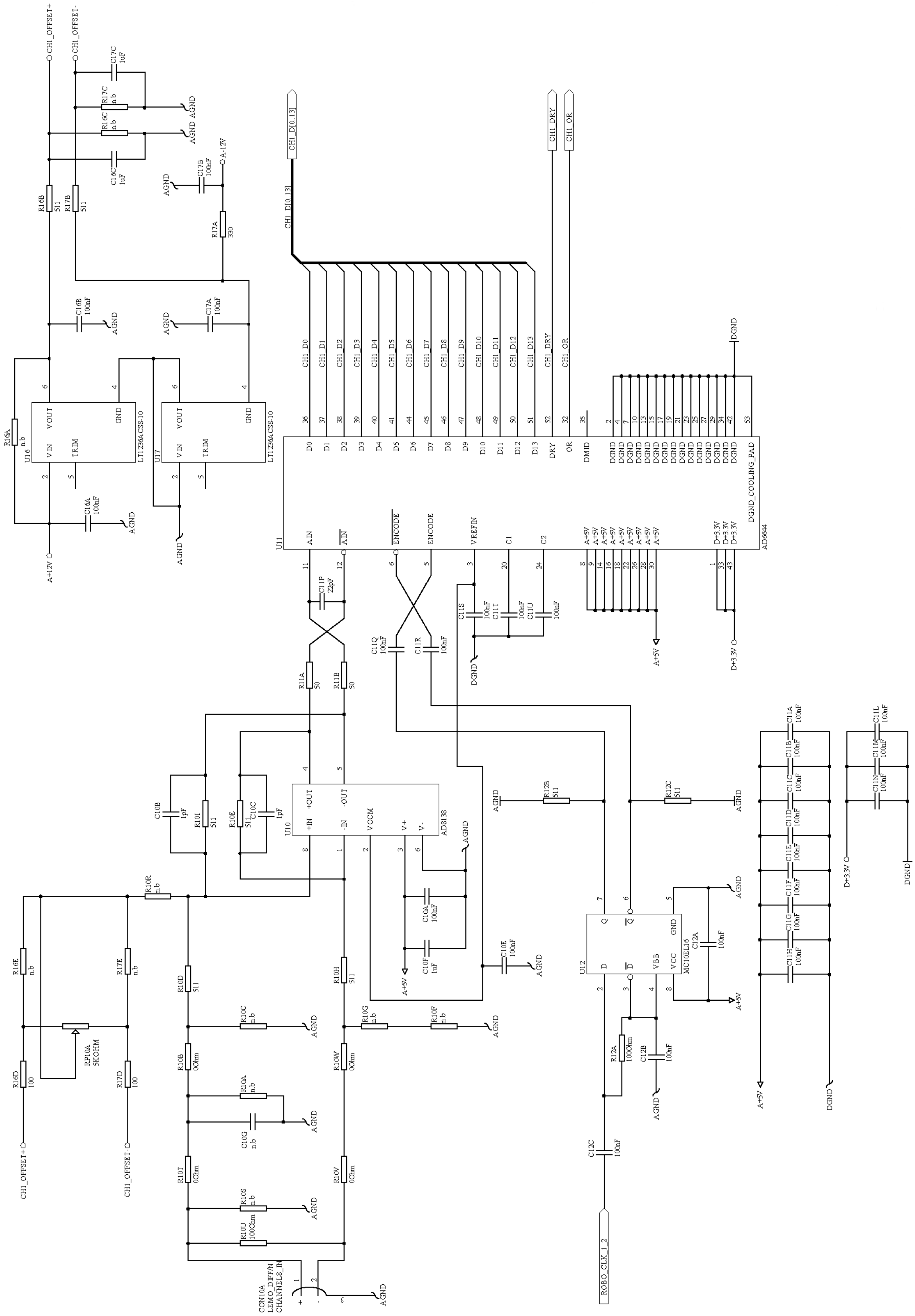
Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

10.7 Input Schematics

10.7.1 SIS330x (single ended)



10.7.2 SIS3301 (differential)



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