AGATA Core- Differential to Single and Pulser CNTRL- NIM Module.

1. Purpose and features

The AGATA-Core NIM Converter Testbed Box was design to perform (simulate) the tasks of the front-end electronics implemented in the AGATA-FADC unit, namely:

- to provide the access to the INH-C1&C2 and SHD-C1&C2 signals, as specified in the AGATA Preamplifier "White Paper" documentation (see, "AGATA Hybrid Preamplifiers with Pulser, Version 2.3 March 2006 (or later) A. Pullia and G. Pascovici)
- to generate the required signal sequences to fully control the Core Programmable Spectroscopic Pulser placed in AGATA Core preamplifier.
- additionally, the module converts the Agata Core preamplifier differential signals into single ended signals (terminated on 50 Ohm) to facilitate potential further comparative tests with other standard commercial multichannel analyzers etc.

2. Description

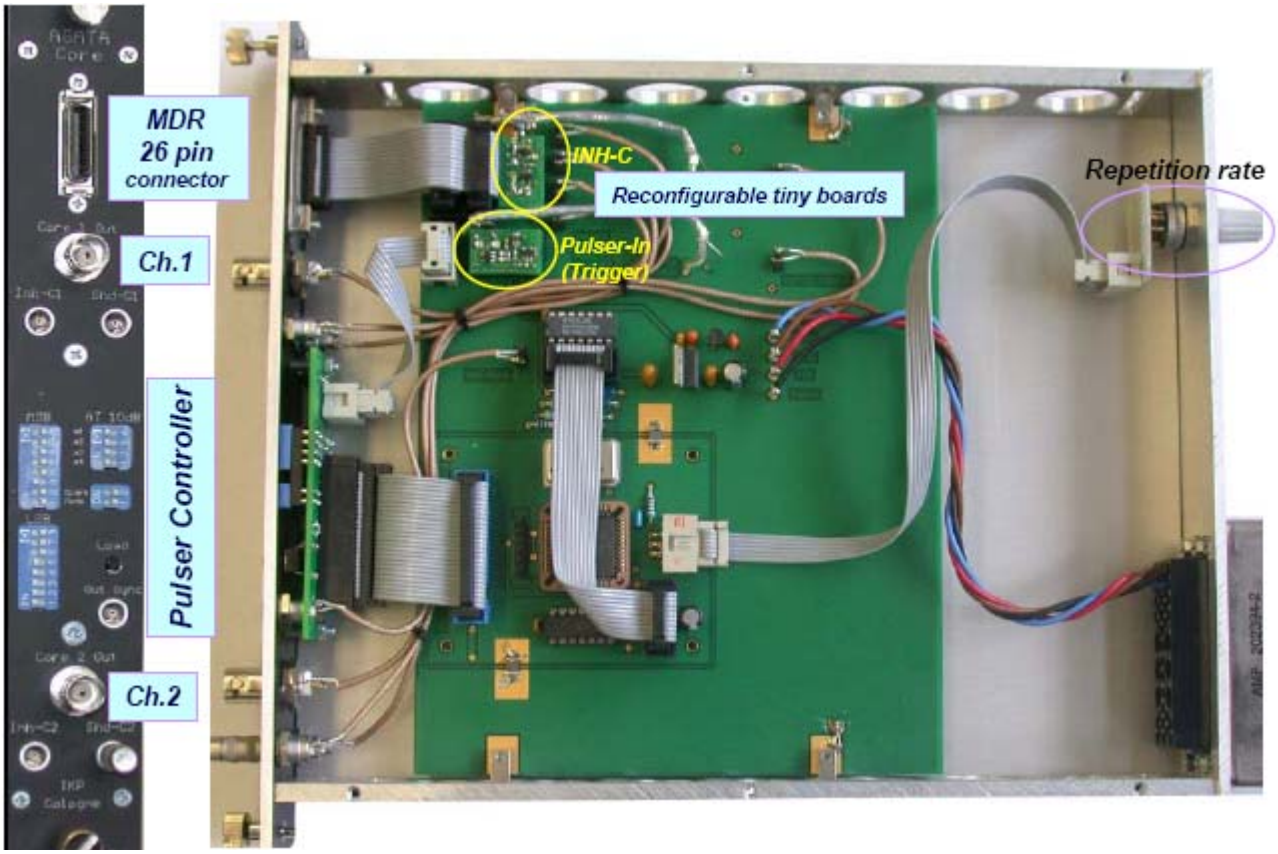


Fig. 1 Layout of the NIM module- with its components right side opened.

The AGATA-Core differential to single ended unit is designed as a standard single-width NIM module. It accepts the input differential linear signals and all digital communication signals coming from or sent to the AGATA-Core preamplifier through MDR multiwire transmission line.

2.1 Differential to Single-Ended signal converter

There are two versions of AGATA-Core preamplifiers, namely with one analog channel (also called “Single Gain Core”) and with two analog channels (also called “Dual Gain Core”) [1, 2] The differential signals are received at the MDR26 front panel connector and converted to single ended signals as shown in Fig.1 (the operational amplifier U5-LM6171A converts the differential signals of the Single Gain Core preamplifier or of the Ch.1 of the Dual Gain Core preamplifier, respectively and the operational amplifier U7-LM6171 converts the differential signals of the Ch.2 of the Dual Gain Core preamplifier). The impedance of the analog output signals is ~50 Ohm, i.e. an external termination with an additional 50 ohm reduces the signal amplitude to ~50%

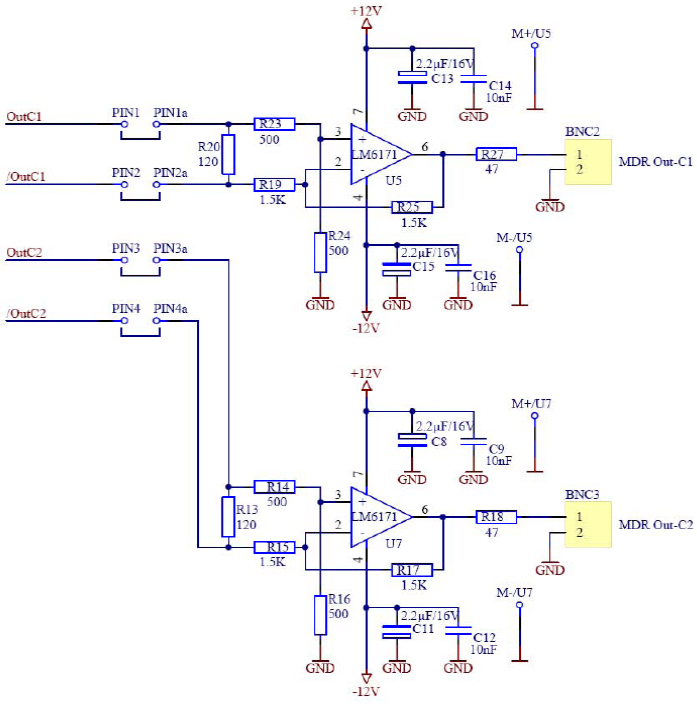


Fig.2 Differential to single ended schematics

2.2 The management of the digital signals: INH-C, Pulser-In(Trigger) and SHDN-C

As described in the AGATA Hybrid Preamplifiers with Pulser (Version 2.3-March 2006) the digital signals **INH-C** and **SHDN-C** of the AGATA Single Gain Core preamplifiers and the first Dual Gain Core preamplifiers are designed and manufactured with LV-CMOS logic for their logic signals. The last version of the AGATA dual gain core preamplifiers is designed in a reconfigurable architecture of the digital signals, accepting either TTL (LV-CMOS) or LV-DS standards for its logic signals. The LV-DS logic was selected in order to attenuate the cross-talk, induced in the 10m long MDR-transmission cable, between the INH-Ch1 digital signal and Core-Ch.2 analog signal and between the Pulser-In (Trigger) digital signal and Core-Ch.1 & Ch.2. analog signals, respectively. ***Therefore, the LV-DS logic standard configuration is the advised set-up to be implemented in AGATA-Core preamplifier and in the front-end electronics of the AGATA-FADC unit.***

Note*: - The present module has also a reconfigurable architecture for its logic signals: INH-C1, INH-C2 and Pulser-In (Trigger). ***The user is strongly advise*** to set the logic standard of these signals ***in the same configuration as the AGATA core preamplifiers are***, at the other end of the MDR transmission cable. To do that, please follow the schematics and solder the jumpers accordingly to selected configuration (see also Fig. 3 and Fig. 4)

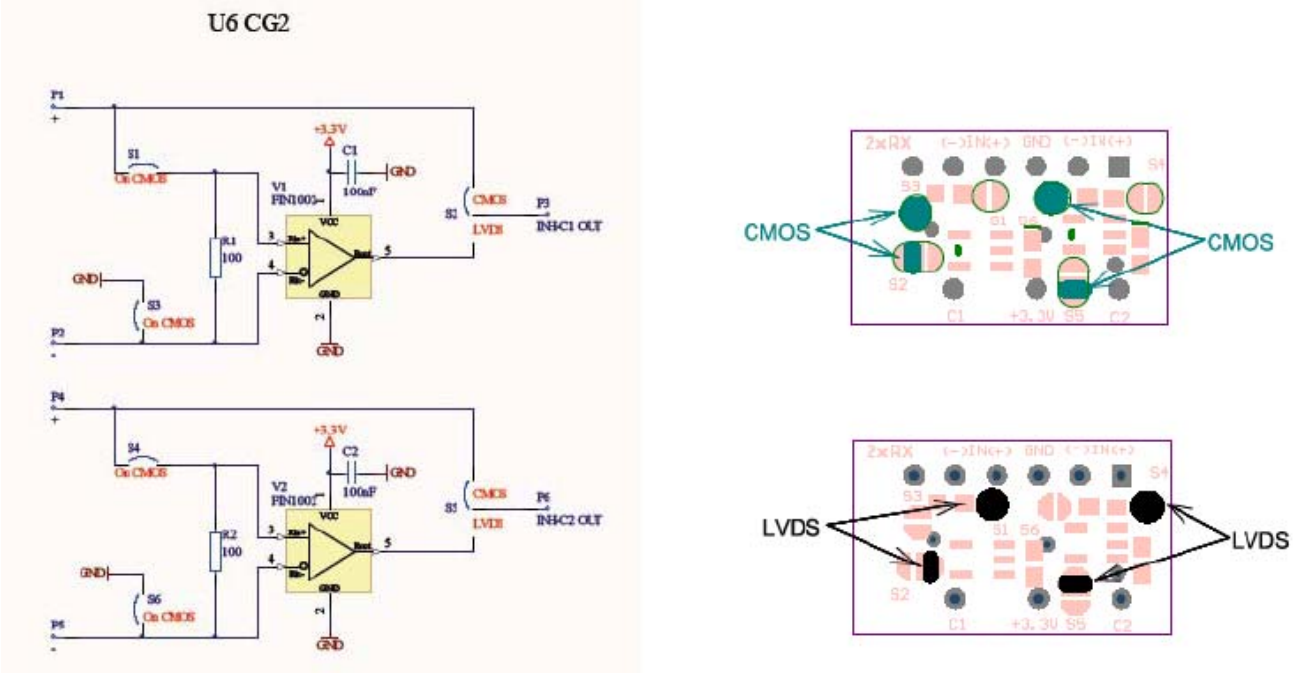


Fig. 3 Schematics and jumper selection for **LV-CMOS** logic or **LV-DS** logic of **INH-C1** and **INH-C2** digital signals

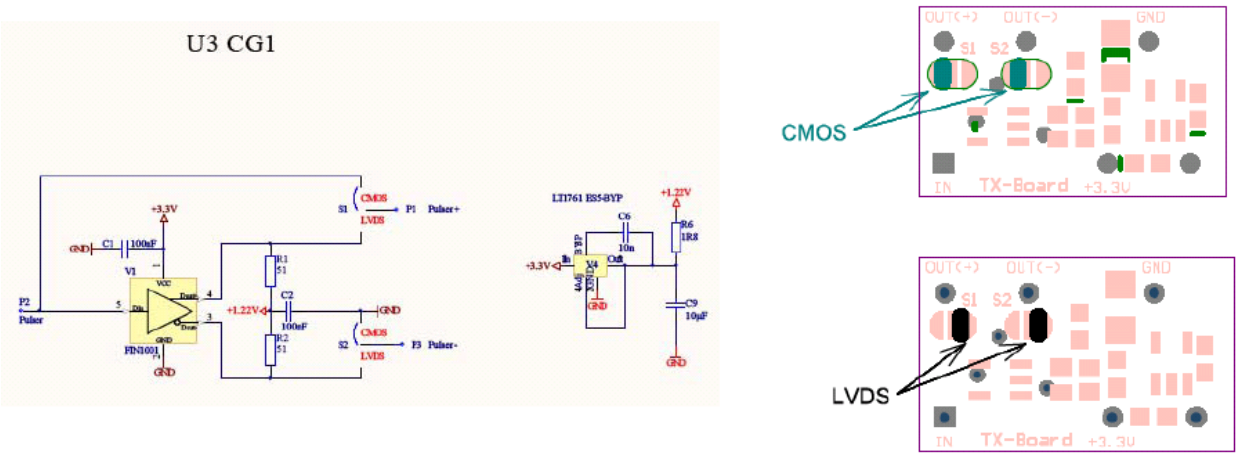


Fig. 4 Schematics and jumper selection for **LV-CMOC** logic or **LV-DS** logic of the **Pulser-In (Trigger)** digital signal

The **SHDN** digital signal is used as control of the fast reset circuitry. It can be used statically or dynamically. If the **SDHN** is low the fast reset works autonomously (e.g. one can keep the SHDN signal low just putting a 50 ohm terminator at its LEMO input connector), if the SHDN signal is high the fast reset circuitry is disabled , i.e. the INH-C output signals are disabled.

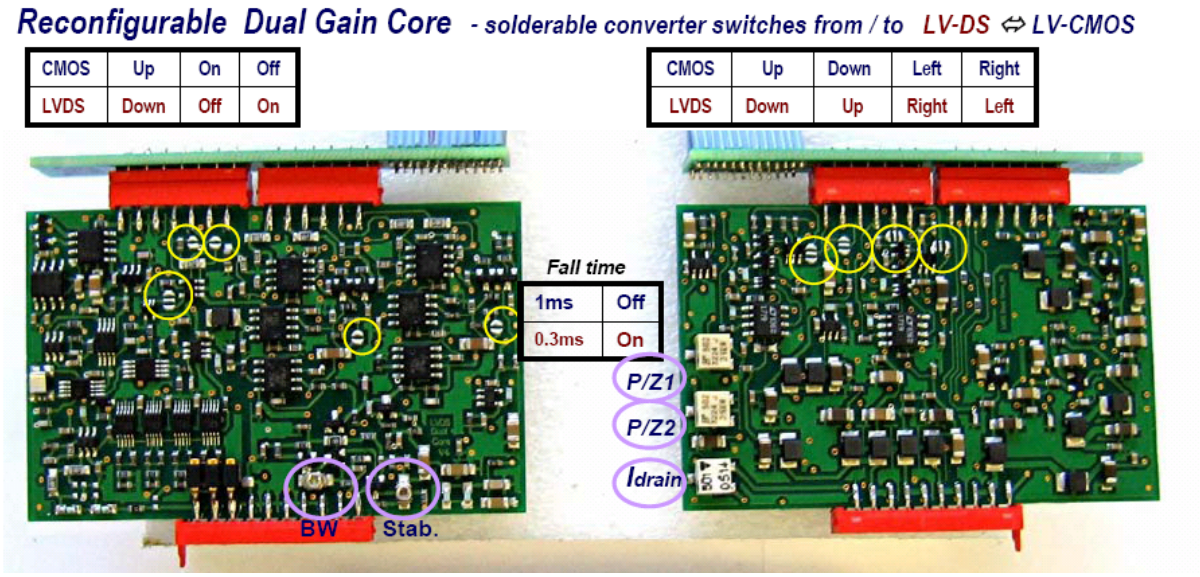


Fig.5 Layout of the AGATA Core Dual Gain Preamplifier (top view-left, bottom view right). The reconfigurable solderable converter switches positions are shown in the attached table (on the top of the pictures) for the CMOS standard logic (blue) and LV-DS standard logic (red).

MDR ⇔ (CSP)	MDR ⇔ (FADC)	Dual Core (LV-DS)	Dual Core (LV-CMOS)	Single Core (CMOS)
1	26	GND	GND	GND
2	25	Core-Ch1-(200mV) ⇔ Pair 1(-)	Core-Ch1-(200mV) ⇔ Pair 1(-)	Core-Ch1-(100mV) ⇔ Pair 1(-)
3	24	AT10_2 ⇔ Pair 2 (-)	AT10_2 ⇔ Pair 2 (-)	AT10_2 ⇔ Pair 2 (-)
4	23	AT10_4 ⇔ Pair 3 (-)	AT10_4 ⇔ Pair 3 (-)	AT10_4 ⇔ Pair 3 (-)
5	22	Mode ⇔ Pair 4 (-)	Mode ⇔ Pair 4 (-)	Mode ⇔ Pair 4 (-)
6	21	GND ⇔ Pair 5 (-)	GND ⇔ Pair 5 (-)	GND ⇔ Pair 5 (-)
7	20	GND ⇔ Pair 6 (-)	GND ⇔ Pair 6 (-)	GND ⇔ Pair 6 (-)
8	19	SHDN-Ch2 ⇔ Pair 7 (-)	SHDN-Ch2 ⇔ Pair 7 (-)	EN-PS ⇔ (N.C.)_GND??
9	18	Pulser-In(-) ⇔ Pair 8 (-)	GND ⇔ Pair 8 (-)	GND ⇔ Pair 8 (-)
10	17	/INH-Ch2(-) ⇔ Pair 9 (-)	GND ⇔ Pair 9 (-)	GND ⇔ Pair 9 (-)??
11	16	/INH-Ch1(-) ⇔ Pair 10 (-)	GND ⇔ Pair 10 (-)	GND ⇔ Pair 10 (-)
12	15	/Core-Ch2-(50mV) ⇔ Pair 11(-)	/Core-Ch2-(50mV) ⇔ Pair 11(-)	N.C. ⇔ Pair 11(-) GND??
13	14	GND	GND	GND
14	13	GND	GND	GND
15	12	Core-Ch1-(200mV) ⇔ Pair 1(+)	Core-Ch1-(200mV) ⇔ Pair 1(+)	Core-Ch1-(100mV) ⇔ Pair 1(+)
16	11	AT10_1 ⇔ Pair 2 (+)	AT10_1 ⇔ Pair 2 (+)	AT10_1 ⇔ Pair 2 (+)
17	10	AT10_3 ⇔ Pair 3 (+)	AT10_3 ⇔ Pair 3 (+)	AT10_3 ⇔ Pair 3 (+)
18	9	Gain-Clk-(DAC) ⇔ Pair 4 (+)	Gain-Clk(DAC) ⇔ Pair 4 (+)	Gain-Clk(DAC) ⇔ Pair 4 (+)
19	8	Gain-Data-(DAC) ⇔ Pair 5 (+)	Gain-Data(DAC) ⇔ Pair 5 (+)	Gain-Data(DAC) ⇔ Pair 5 (+)
20	7	/Gain-Select-(DAC) ⇔ Pair 6 (+)	/Gain-Select(DAC) ⇔ Pair 6 (+)	/Gain-Select(DAC) ⇔ Pair 6 (+)
21	6	SHDN-Ch1 ⇔ Pair 7 (+)	SHDN-Ch1 ⇔ Pair 7 (+)	SHDN-Ch ⇔ Pair 7 (+)
22	5	Pulser-In (+) ⇔ Pair 8 (+)	Pulser-In (+) ⇔ Pair 8 (+)	Pulser-In (+) ⇔ Pair 8 (+)
23	4	INH-Ch2(+) ⇔ Pair 9 (+)	INH-Ch2 ⇔ Pair 9 (+)	GND ⇔ Pair 9 (+)??
24	3	INH-Ch1(+) ⇔ Pair 10 (+)	INH-Ch1 ⇔ Pair 10 (+)	INH-Ch ⇔ Pair 10 (+)
25	2	Core-Ch2-(50mV) ⇔ Pair 11(+)	Core-Ch2-(50mV) ⇔ Pair 11(+)	N.C. ⇔ Pair 11(+) GND??
26	1	GND	GND	GND

Table 1 MDR-26pin connector - Pin assignments at the charge sensitive preamplifier end (yellow) and at the AGATA-FADC-Unit and present NIM module end (green). All potential configurations of the AGATA-Core Charge Sensitive Preamplifier & Pulser board are shown.

2.3 AGATA-Core Programmable Spectroscopic Pulser (PSP) Controller

2.3.1 AGATA – Core PSP Specifications

Pulse type - Rectangular or Tail pulse
Polarity - Positive in Rectangular mode
- Positive/Negative in Tail mode
External Trigger - 0 to 500 c.p.s. Periodic or Statistical,
Threshold selectable, either CMOS logic or LV-DS (with Eos~1.25V)
Resolution - 16 bit
Jitter - +/- 10 ppm

2.3.2 PSP- Controller

The PSP-Controller part of this NIM module was designed to simulate the functionality of the AGATA-FADC and Pre-processing units. The main features of this SPS-Controller are: - to set the desired amplitude, -repetition rate and -mode of operation of the PSP integrated in the AGATA-Core Charge Sensitive Preamplifier at the other end of the MDR-cable assembly.

A) Pulse amplitude

The pulser amplitude can be controlled by three sets of binary SIL switches (K1, K2 and K3) and one push-button (T1).

The first two SIL x 8 positions switches K1 and K2 correspond directly to the DAC's binary 16 bits, namely the K1-(above) to the MSB and the K2-(bellow) to the LSB.

The four positions switch K3 corresponds to a four step attenuators of x10dB each, i.e. a maximum attenuation factor of x100.

- Programming the 16 bit Serial DAC (type AD5451C)

The communications channel requires a 3-wire industry standard interface consisting of a Clock signal, a data signal and synchronization signal. The AD5541C DAC requires a 16-bit data word with data valid on the rising edge of serial clock signal (SCLK). The DAC update cycle is started by the synchronization signal (CS/) which is manually initiated by the bush-button (T1)

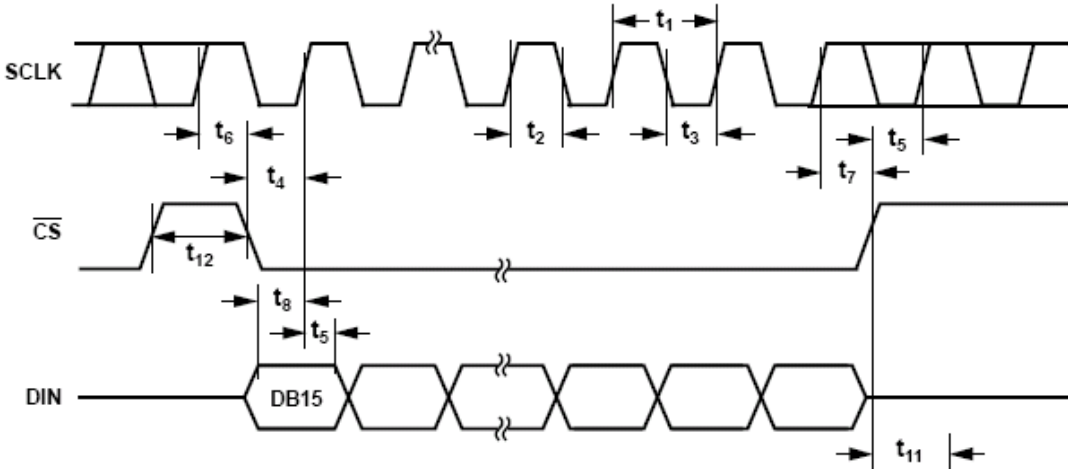


Fig.5 Timing of the communication channel between the 16 bit serial DAC placed in the AGATA-CSP and the AGATA-Core NIM programming module

Note* In order to get best signal/noise ratio, the user is advised to set in logic "1" at list one of the first four MSB (K1-above) of the DAC and to activate the attenuator switches (K3) to get smaller amplitudes.

- Attenuators

The four step attenuator consists of four independent attenuators, each with 10 dB attenuation factor. The attenuator is not synchronized with the DAC update cycle, it is simple DC coupled.

B) Clock and Repetition Rate

The repetition rate of the PSP as well as the timing of the DAC update cycle is generated by an internal quartz clock and a small programmable chip (Altera-EPM7064SLC44).
The repetition rate can be changed from a switch placed on the rear panel.
One can select between:

- 0 Hz – i.e. the Programmable Spectroscopic Pulser in AGATA-Core CSP is disabled
- 50; 100 or 200 Hz (or alternatively: 100; 200 or 400Hz, by request)

C) Mode of operation

The user can select between Rectangular Pulses or Exponential Tail Pulses by turning the K4/1 switch: -left- for the Rectangular, -right- for the Exponential Tail, respectively.

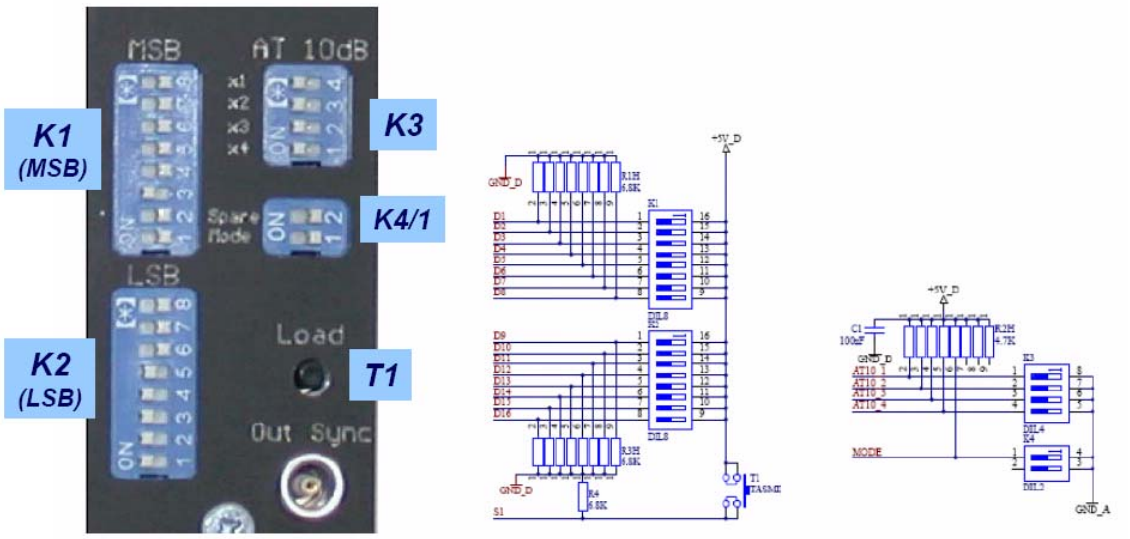


Fig.6 Front panel PSP programming switches (K1, K2, K3, K4) and push-button (T1)

*Note for the file *)*
How to perform Time over Threshold (ToT) spectrometry with this module

When one of the AGATA-Core spectroscopic channel's amplitude is larger than the comparator threshold (~1V amplitude, i.e. very closed to the ADC saturation point), one gets a large saturated pulse at its analog spectroscopic output and one CMOS logic signal at the **INH-C** output, i.e. at the output of related comparator.

In principle, in ToT mode of operation, the width of the **INH-C** signal (**T**) contains the whole spectroscopic information, the width **T** being proportional with the collected charge at the central electrode. The range of the reset time-interval (**T** in Fig. 7 right) is about ~1-12 μs and the accuracy of

the ToT method is closed to ~0.1%. That means, to perform a precise measurement, one has to use a simple universal time interval counter device, with less than 1 ns intrinsic time resolution for pulse width or time-interval measurements. For example, such device could be the Universal Time-Interval Programmable Counter **GTX2230 PXI** board. If it is programmed in "Pulse Width" mode of operation, defining Pulse polarity "Positive" and a sequence of "Positive/Negative Slopes" then it could provide a convenient way to measure the pulse width of the **INH-C** signal, with ~100 ps time resolution

As presented in [3], one can **extend more accurately the spectroscopic range** well above the ADC dynamic range analyzing the digitized histograms of two pulses, namely of the analog signal at the output of the AGATA-Core charge sensitive preamplifier and logic signal INH-C. The first signal is needed while the saturated analog signals of the charge sensitive preamplifier could be superposed to the exponential form tail of a previous analog signal (**V**1 in Fig. 7 left) and calculating more accurately the relation between the total energy that is subject to reset (**E**) and its related reset interval-time (**T**) a nonlinear form was found [4], namely:

$$E = b_1 T + b_2 T^2 - k_1 (V_1 - V_2) + E_0$$

Therefore all three experimental values are needed to perform an accurate experimental measurement in Time over Threshold (ToT) mode of operation: **T, V1** and **V2** (Fig. 7).

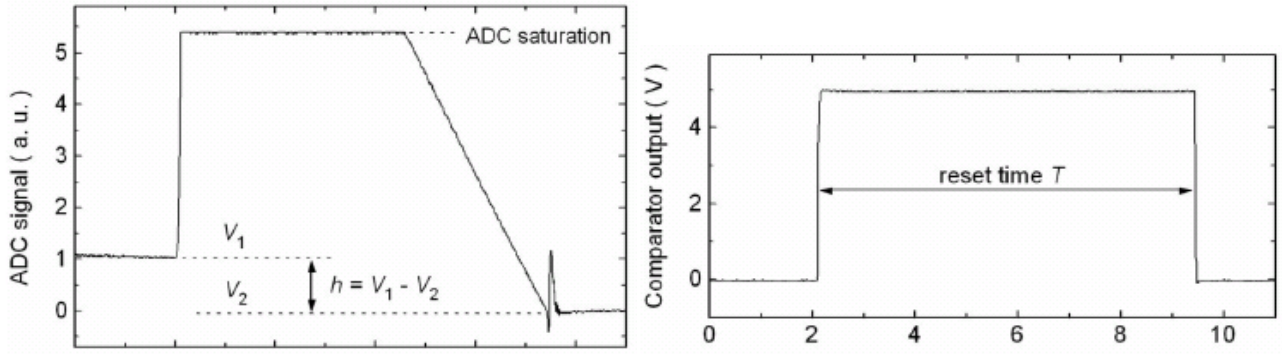


Fig. 7 Left- large signal waveform at the spectroscopic output superposed to the tail of a previous event (V1), showing a flat top at the ADC saturation level.
Right- the comparator logic output signal, the width proportional with the signal amplitude above the threshold

If the AGATA-FADC (with its equivalent 2.4 GHz internal oscillator) is not available for such test measurements then one of the commercial high-speed digitizers with at least 1 GHz clock rate could be used, e.g. one of the following fast digitizers could be good candidates:

- **Agilent U1062** with 4 GHz clock rate in interleaved sampling mode and large input voltage range, accepting directly also CMOS standard logic signals or
- **NI PXI-5153** in interleaved sampling mode with 2 GHz clock rate

Bibliography

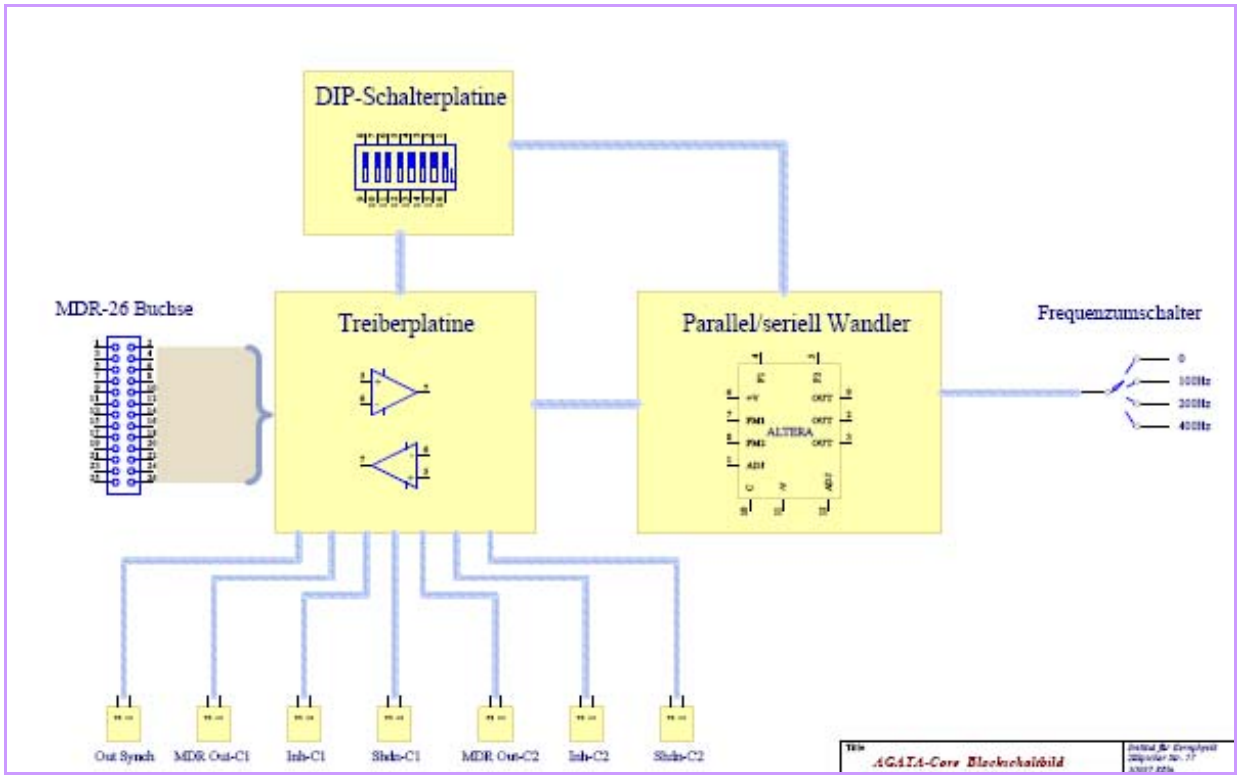
[1] A. Pullia, G. Pascovici, AGATA Hybrid Preamplifiers with Pulser, Vers. 2.3 -March 2006

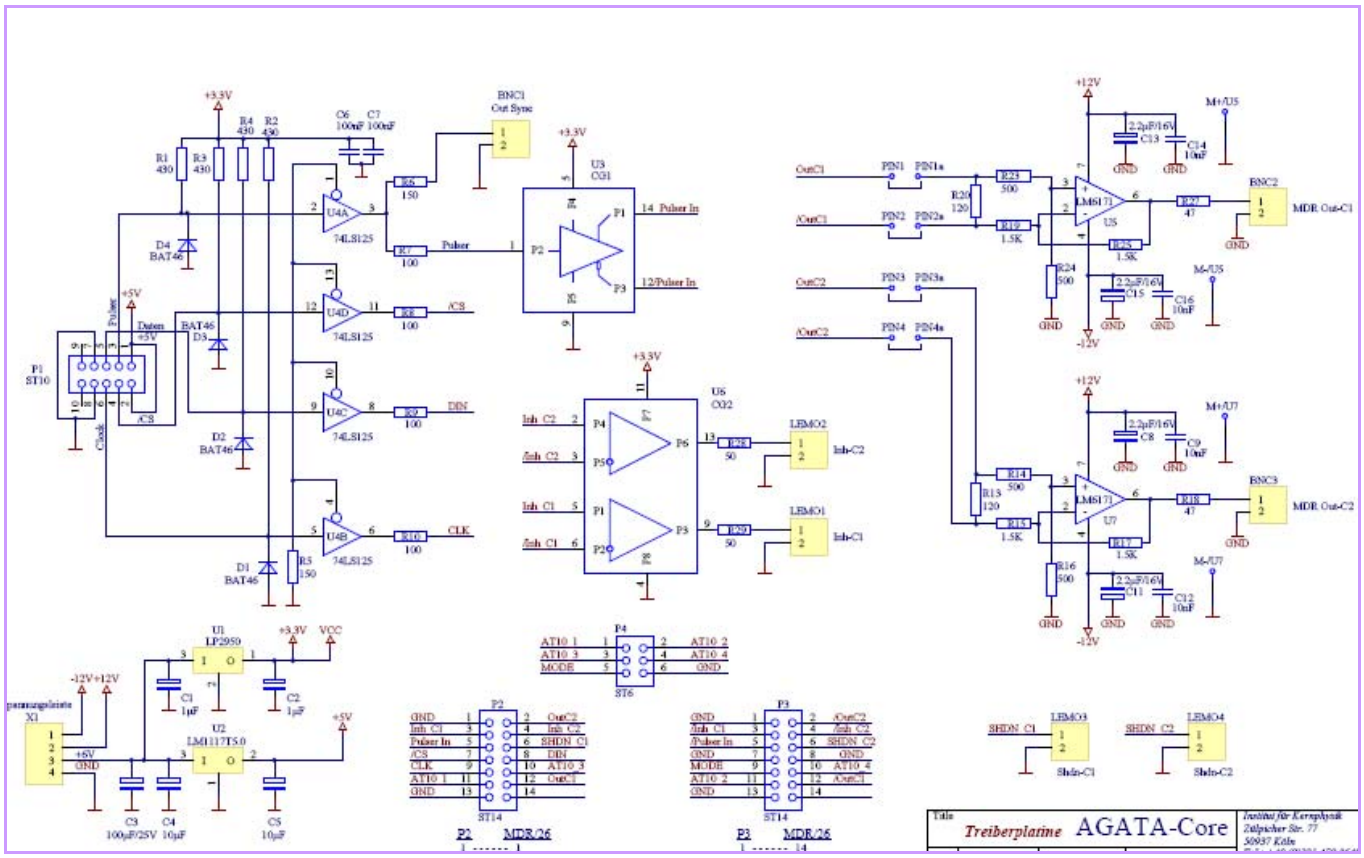
[2] G. Pascovici et al., Low noise, dual gain Preamplifier with built in spectroscopic pulser for highly segmented High-purity germanium detectors, WSEAS Trans. on Circuits & Systems, Vol.**7**, Issue 6, (2008), 470-481

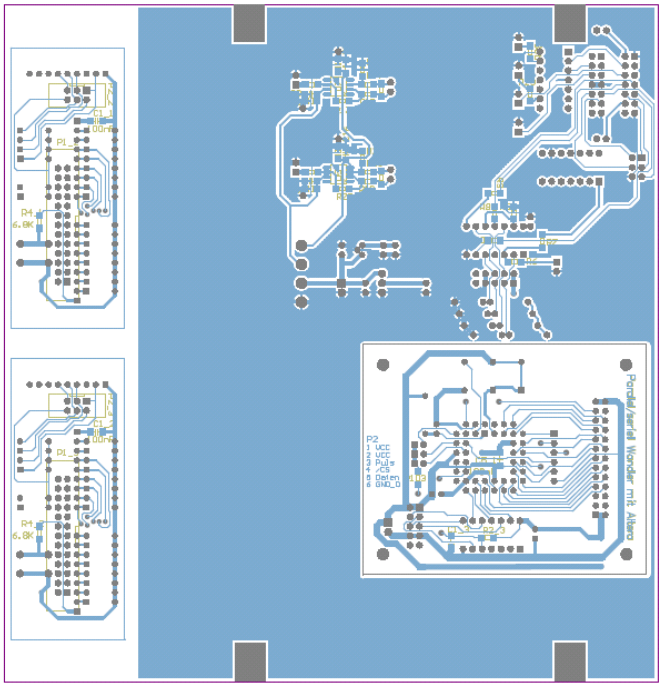
[3] A. Pullia et al., Extending the dynamic range of nuclear pulse spectrometers, Rev. Sci. Instr. **79**, 036105 (2008)

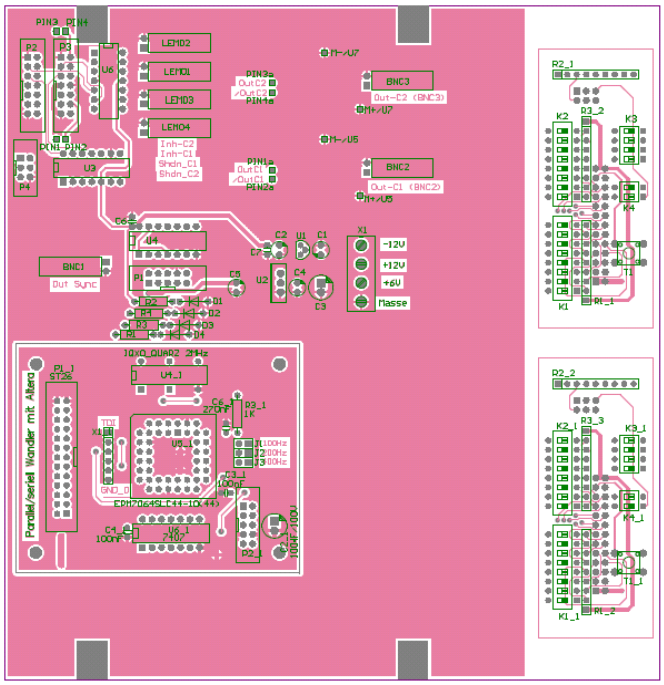
[4] F. Zocca, PhD Thesis, New technologies for low-noise wide-dynamic range preamplification of HPGe segmented detector signals, Univ. of Milan (2008)

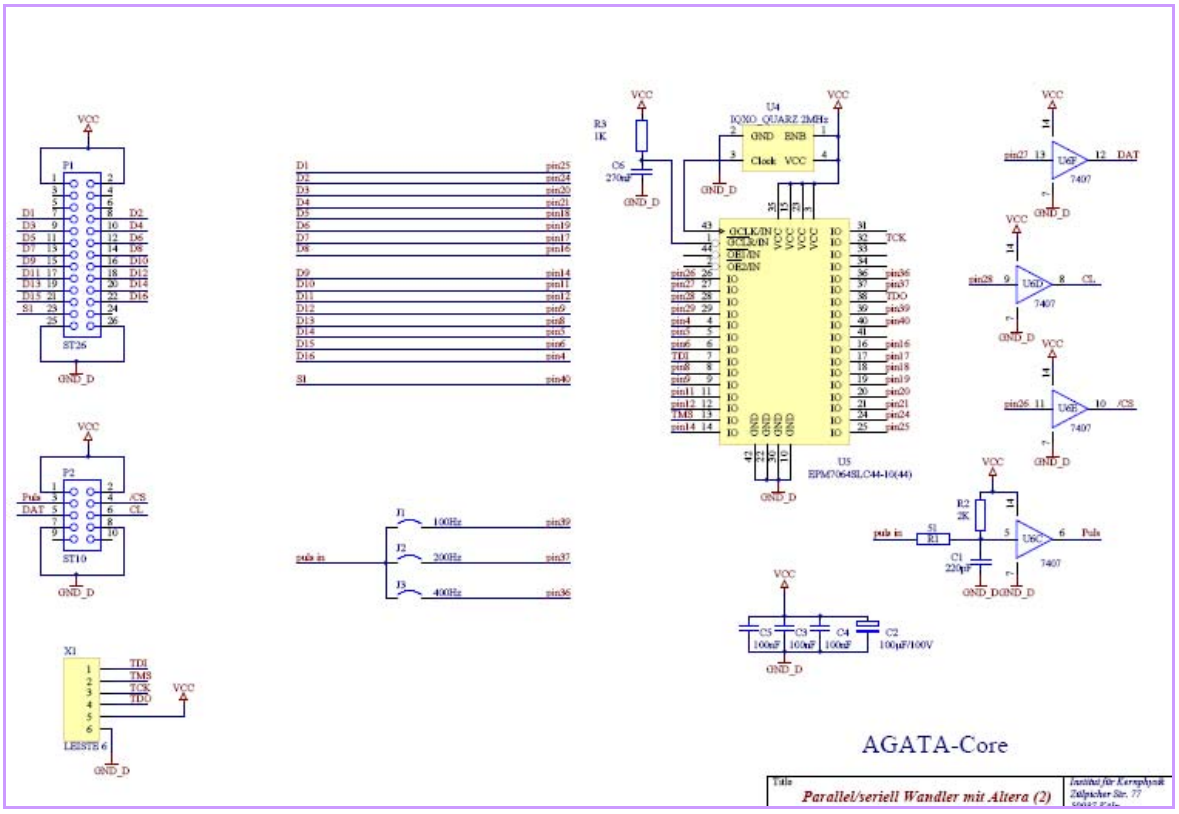
3) Block diagram, Schematics and PCB Layout

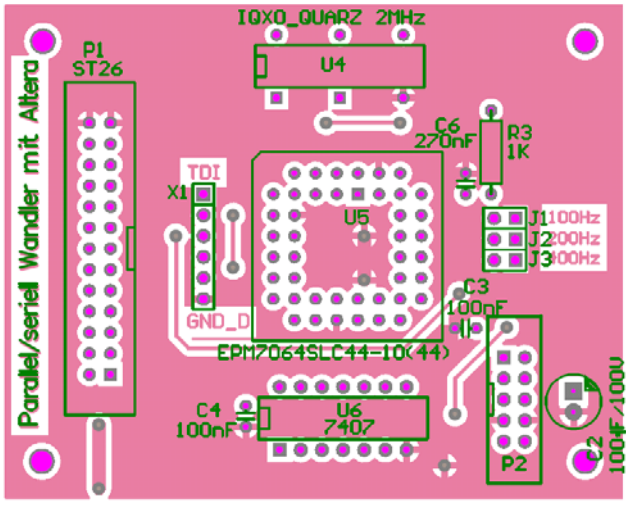


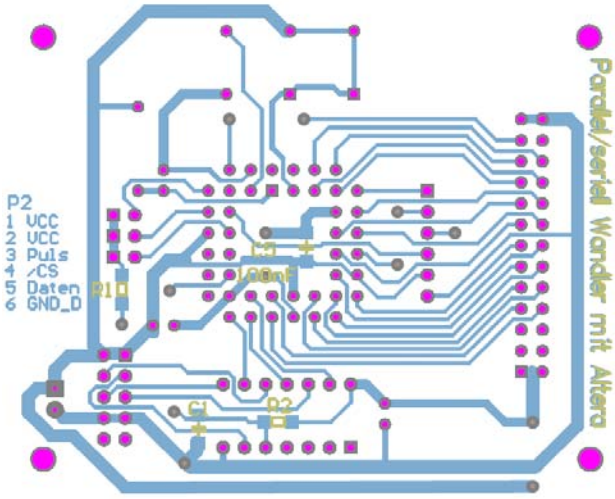



Parallel/serial Wonder mit Albera


LEMO2
LEMO1
LEMO3
LEMO4
BNC3
BNC2
BNC1
Out Sync
-12V
+12V
+6V
Masse
Parallel/serial Wonder mit Albera







Designed and manufactured by Elektronikwerkstatt, IKP, Universität zu Köln,
"AGATA-Core NIM Test Module" (mail to: Elektronik@ikp.uni-koeln.de)